Take-Home Exam: Advanced Hardware (Spring 2007) / Dr. Guy Even

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Solve either one of the design tasks or *both* theoretical questions.

Submission deadlines: deadlines are as follows.

1. Theoretical questions: submit your answers by Aug 12th. Meet me for grading before August 16.
2. Design tasks: submit a plan describing the components of your design by Aug 17th. Complete the task by Sept 17th.

Grading policy: I will grade your exam in your presence. Please come prepared to our meeting! Students who solve the questions are expected to be able to explain their answers. Students who prepare the design are expected to be able to explain the results of the simulations and synthesis.

Citation policy: You may rely on scientific publications and the Internet. You must clearly cite every reference you use.

Cooperation: You are expected not to cooperate with other people. Please respect this rule!

1 Design Tasks

The goal in the design tasks is to acquire a deep understanding of a nontrivial module in a floating point unit.

1. Theoretical questions:
2. Design tasks: Your grade will be mainly based on the quality of the design

2 Design Tasks

The goal in the design tasks is to acquire a deep understanding of a nontrivial module in a floating point unit. grade will be also based on your ability to explain your answer. Interested students can extend the task to a master's project.

2.1 Reciprocal Approximation

Design a parametric design that is given a normalized significand $B \in [1, 2)$ in binary representation. The design outputs X - a representation of an approximation of $1/B$.

The parameter $\varepsilon > 0$ specifies an upper bound on the absolute value of the relative error $|(1/B - X)/(1/B)|$.

Guidelines:

1. Your design should be tailored for values of ε in the range $[2^{-5}, 2^{-23}]$. Namely, one specific design will not do. You should have a separate design for different values of ε. It suffices to consider only values of $\varepsilon = 2^{-i}$ where $5 \leq i \leq 23$.

2. Your design should implement one of the algorithms that appears in the references [Sei99, POMB05, DdD, LA03, Mat01, WIS05, ITY97]. Please coordinate which algorithm you design with me!

3. The design may output the reciprocal approximation in redundant format (carry-save or borrow save) since it is usually fed to a Booth recoded multiplier.

4. Your design should be in VHDL/Verilog.

5. You should run exhaustive simulations of your design for $\varepsilon = 2^{-i}$, where $i \leq 20$.

6. You should synthesize your design for a target FPGA and report timing and hardware requirements for $\varepsilon = 2^{-i}$, where $i \leq 23$.

2.2 Booth Radix 8 Multiplication

Write a generator that is given integer parameters n_1 and n_2 and outputs a Verilog/VHDL description of a Booth Radix 8 multiplier that multiplies two binary numbers whose lengths are n_1 and n_2, respectively.

Guidelines:

1. Reference [EL04] contains a description of a Booth multiplier. Pay special attention to the limited number of bits needed to sign extend the addends in the addition tree.

2. Test your design by executing simulations for multipliers of different sizes. (Aim for millions of test vectors).

3. Synthesize your design for the following values of n_1 and n_2: $(24, 24)$, $(53, 53), (30, 27), (57, 62), (62, 30)$. For each pair, report the timing and hardware requirements.

3 Theoretical Questions

1. Find a polynomial algorithm that solves the following problem:

   Input: A tree $T = (V, E)$ of degree at most 4.

   Output: A layout of T on a square two dimensional unit grid of area $O(|V|)$.

   (a) Describe your algorithm.

   (b) Prove its correctness.

   (c) What is your constant behind $O(|V|)$?

2. Find a combinational circuit with the following properties:

   Input: Two integers x, y in binary representation of length n.

   Output: A binary representation of $\lfloor x/y \rfloor$.

   Delay: The delay of the circuit should be logarithmic in n (the number of bits in the representation of x and y).

   Note: the delay of the circuit taught in class is $\Theta(\log^2 n)$.

References

[DdD] J. Detrey and F. de Dinechin. Table-based polynomials for fast hardware function evaluation. *16th Intl Conference on Application-specific Systems, Architectures and Processors.*

[EL04] M.D. Ercegovac and T. Lang. *Digital Arithmetic.* Morgan Kaufmann Publishers San Francisco, CA, 2004.

[ITY97] M. Ito, N. Takagi, and S. Yajima. Efficient initial approximation for multiplicative division and square root by a multiplication with operand modification. *IEEE Transactions on Computers*, 46(4):495–498, 1997.

[LA03] T. Lang and E. Antelo. Radix-4 reciprocal square-root and its combination with division and square root. *Computers, IEEE Transactions on*, 52(9):1100–1114, 2003.

[Mat01] D.W. Matula. Improved Table Lookup Algorithms for Postscaled Division. *Proc. 15th Symp. Computer Arithmetic (ARITH15)*, pages 101–108, 2001.

[POMB05] J.A. Pineiro, S.F. Oberman, J.M. Muller, and J.D. Bruguera. High-speed function approximation using a minimax quadratic interpolator. *IEEE Transactions on Computers*, 54(3):304–318, 2005.

[Sei99] P.M. Seidel. High-speed redundant reciprocal approximation. *INTEGRATION, the VLSI Journal*, 28:1–12, 1999.

[WIS05] E.G. Walters III and M.J. Schulte. Efficient Function Approximation Using Truncated Multipliers and Squarers. *Proceedings of the 17th IEEE Symposium on Computer Arithmetic (ARITH'05)-Volume 00*, pages 232–239, 2005.