Shimon Even

June 15, 1935 - May 1, 2004

Chapter 11: Flip-Flops

Computer Structure
&
Intro. to Digital Computers

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Tel-Aviv Univ.

Goals

- introduce clock signal.

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- define edge-triggered flip-flops.

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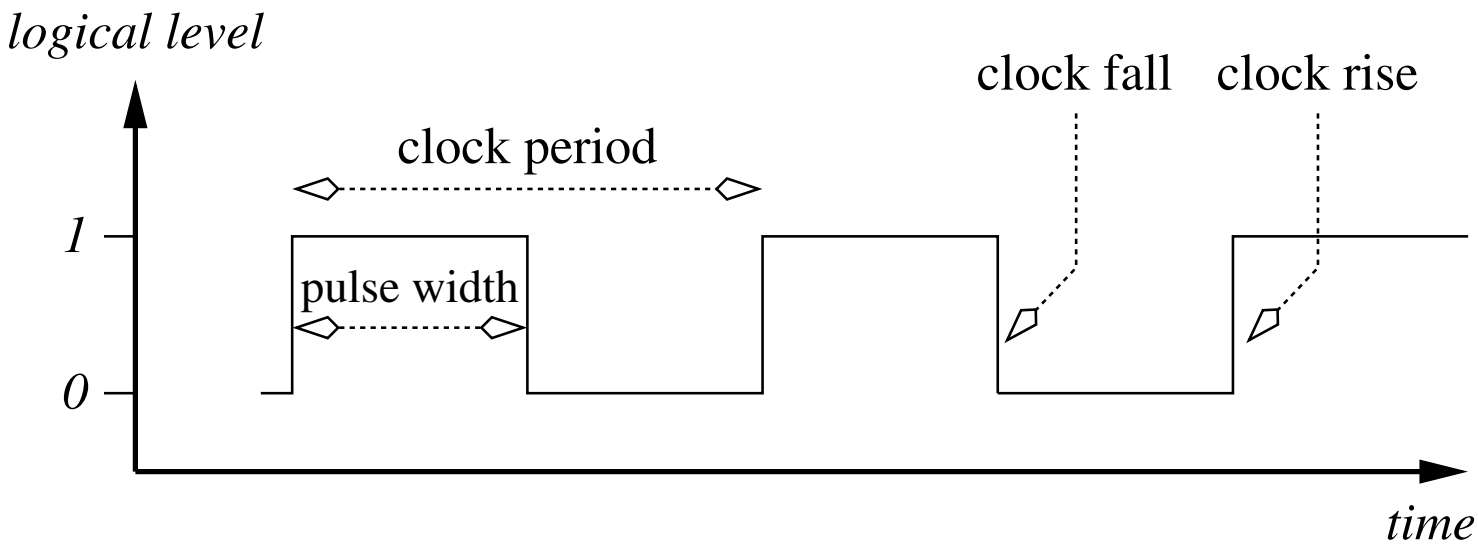
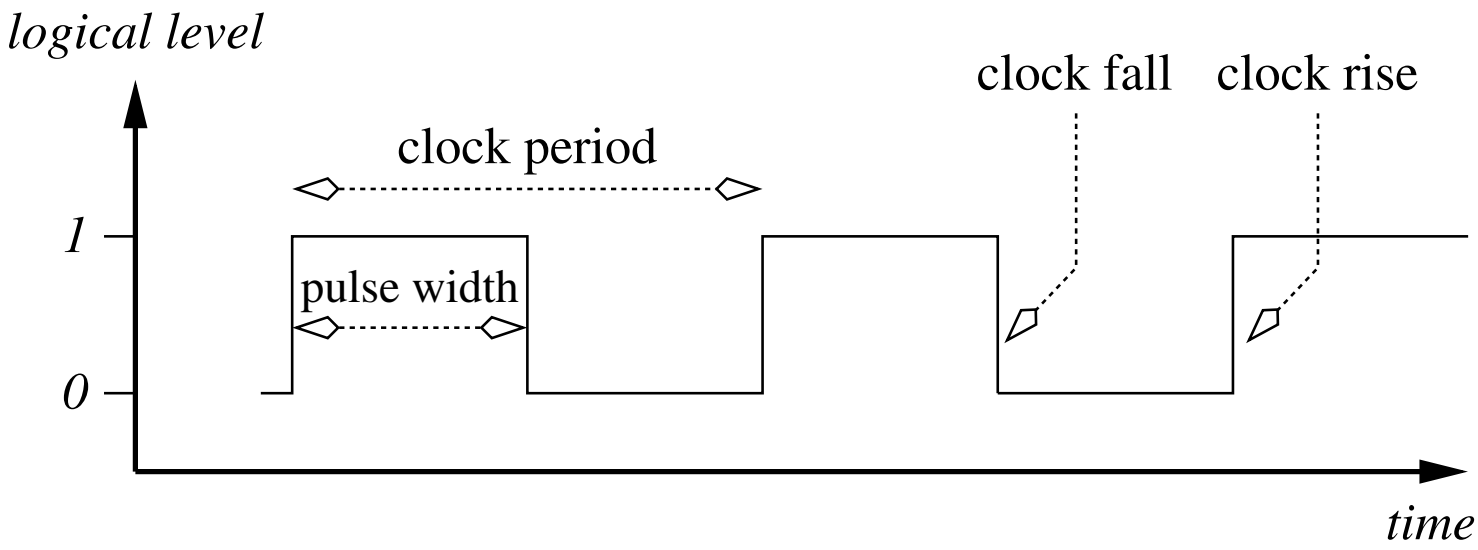
- explain importance of critical segment.
- understand timing of a flip-flop.
- other memory devices.

The Clock


logical level
clock fall
clock rise
clock period
1
pulse width
0
time

The Clock



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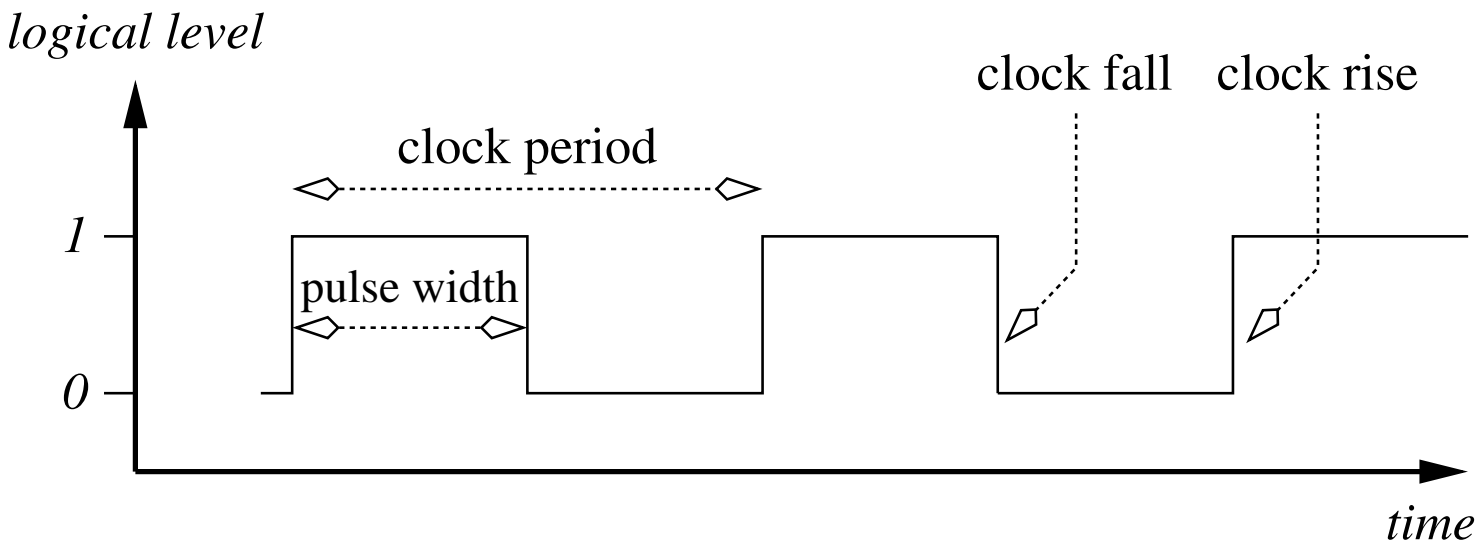

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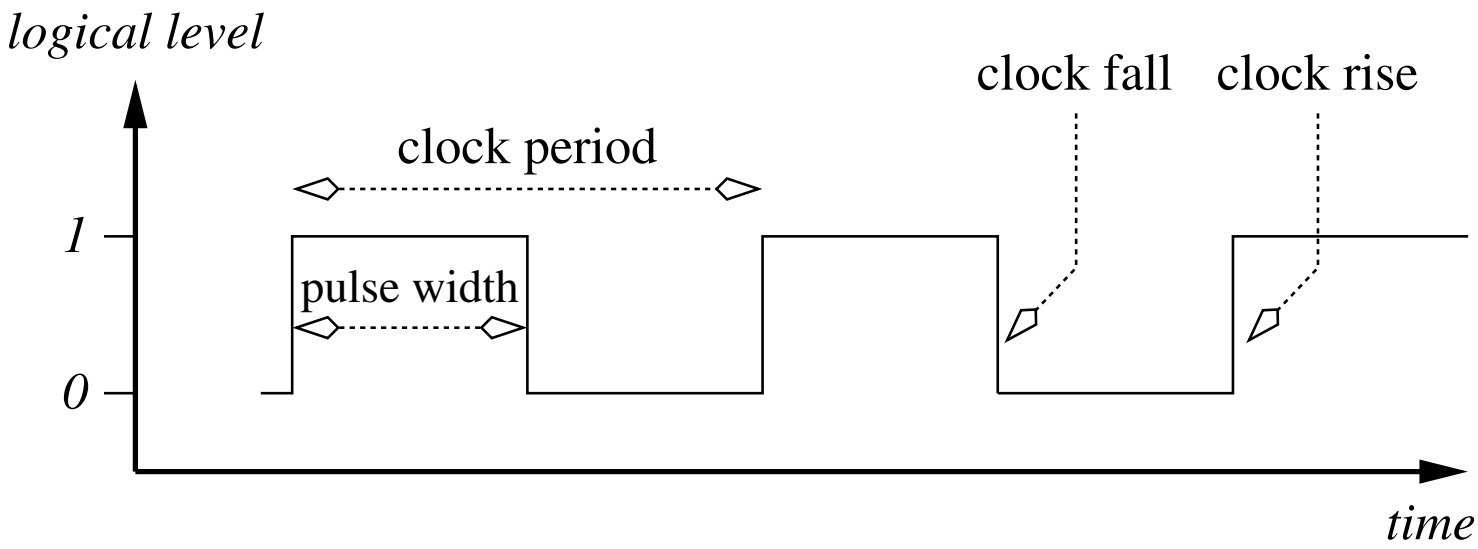

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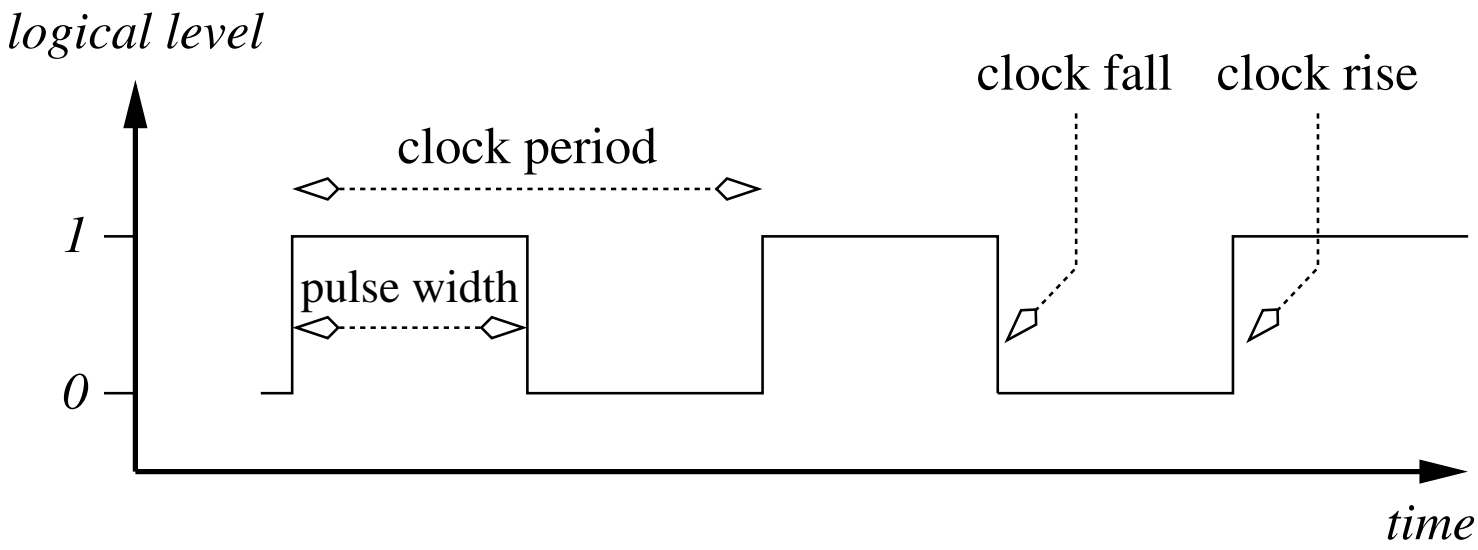

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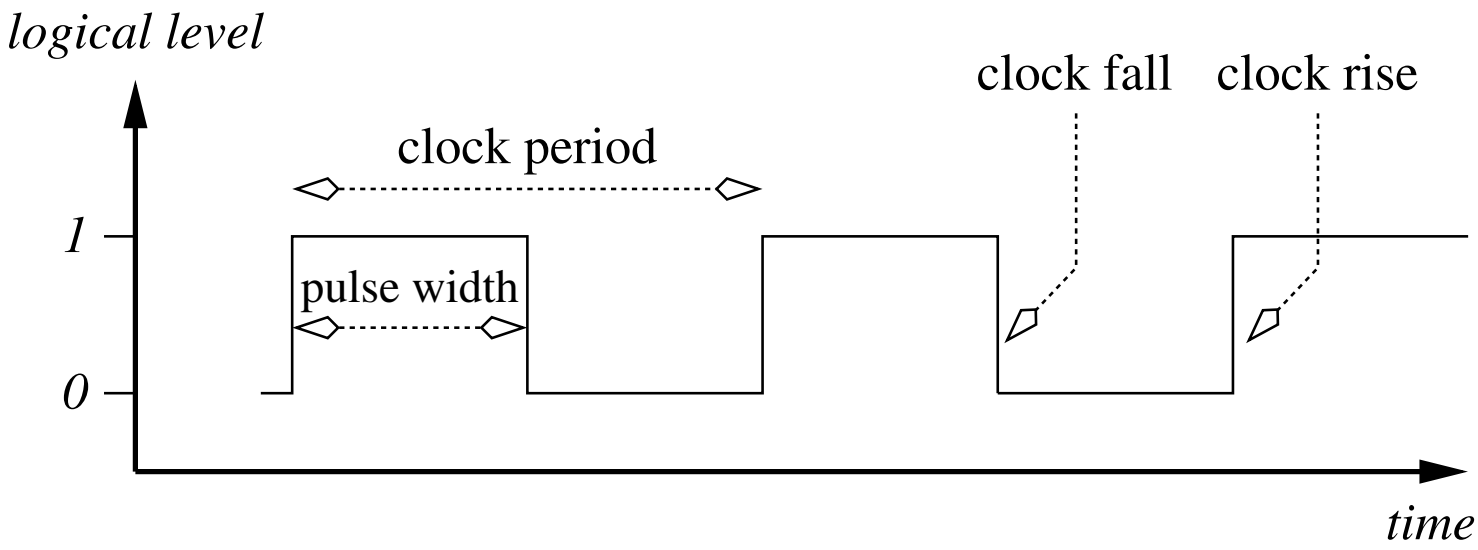

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- we denote the clock signal by CLK.

Clock terminology

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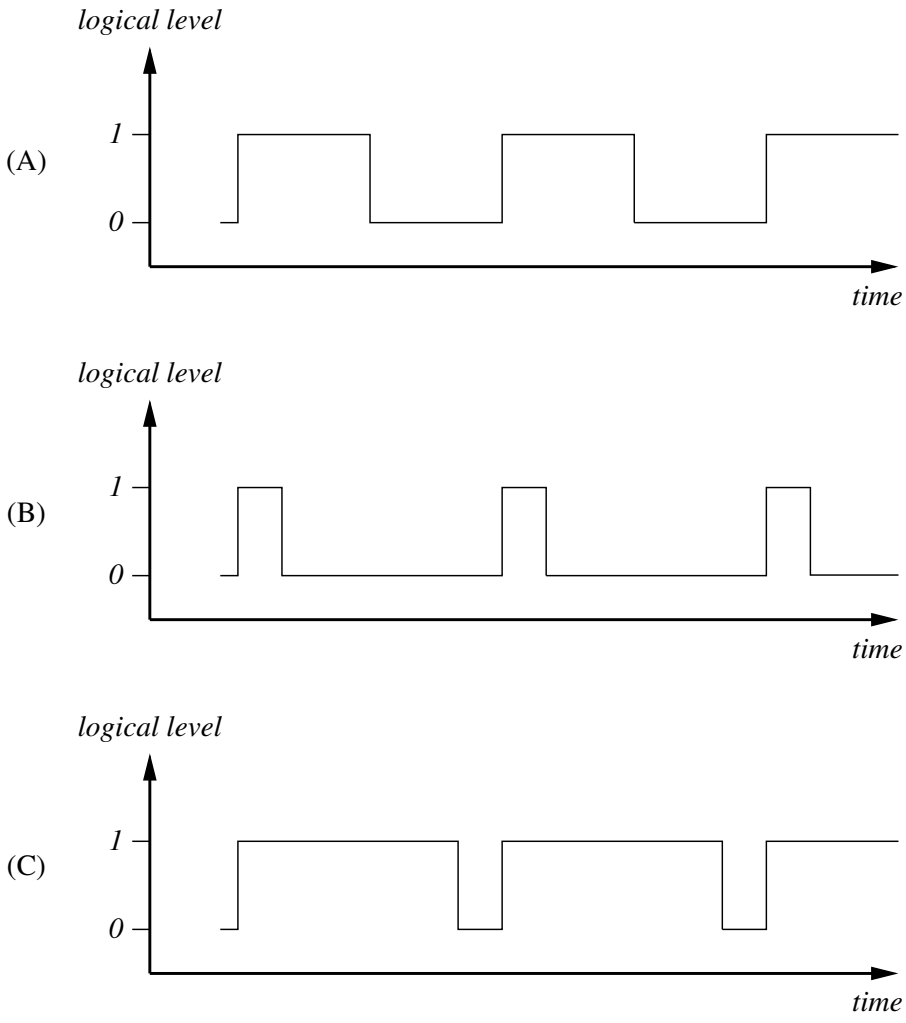

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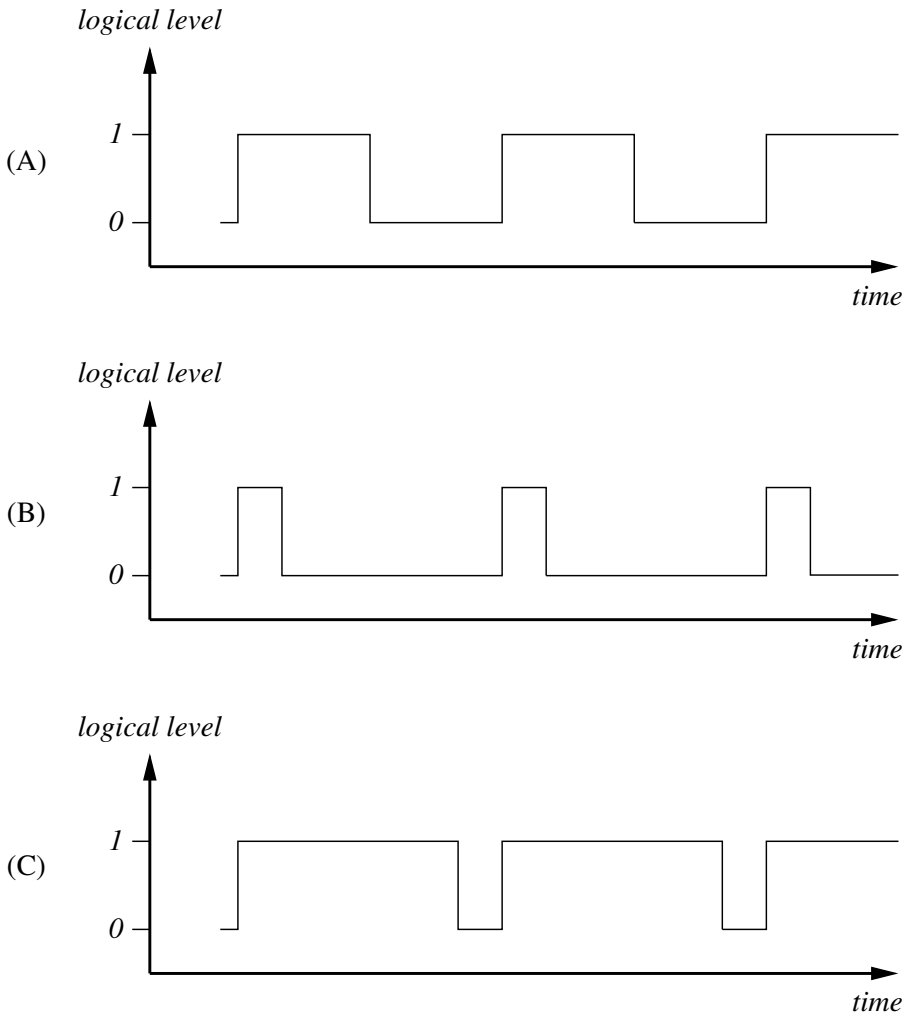

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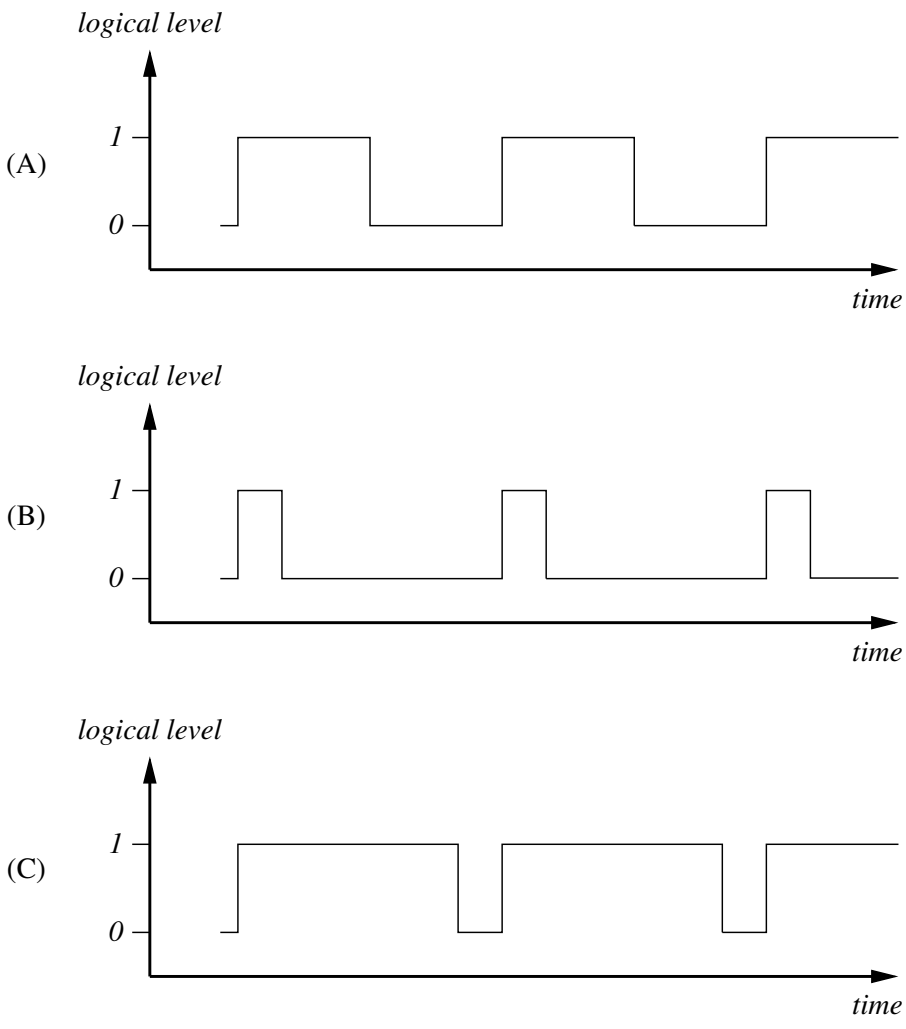

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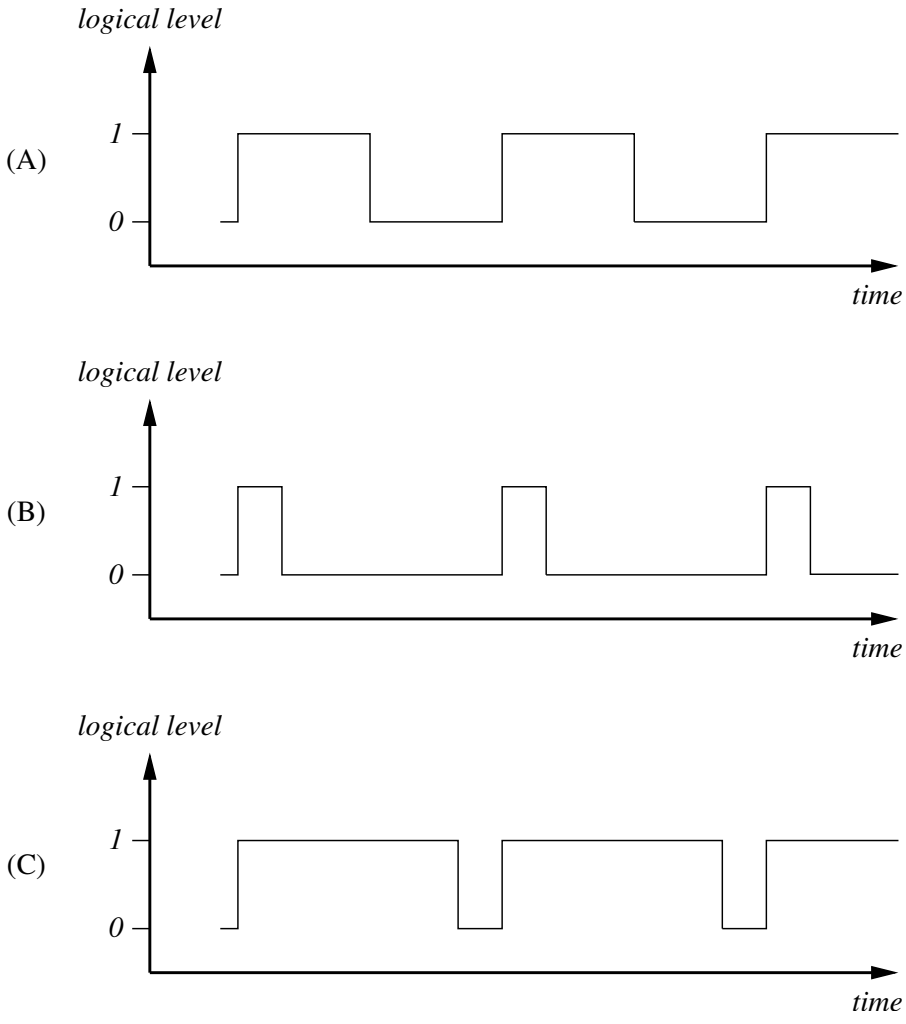

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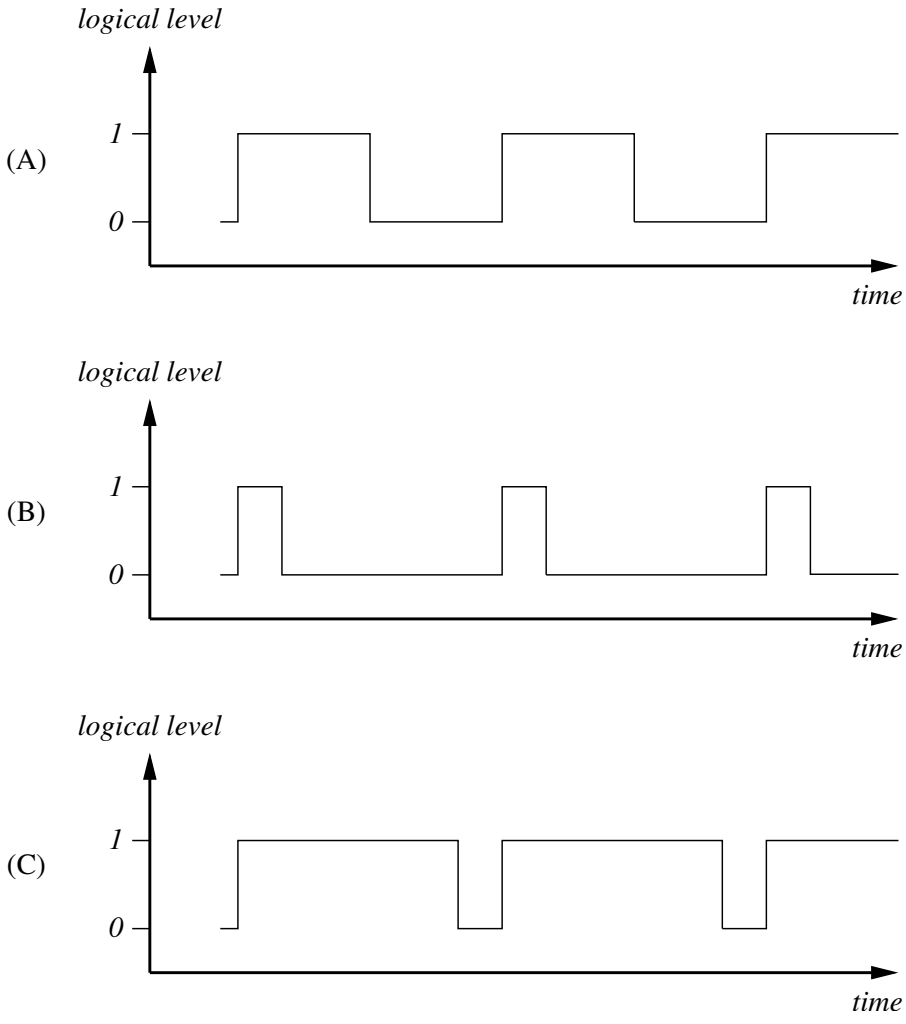

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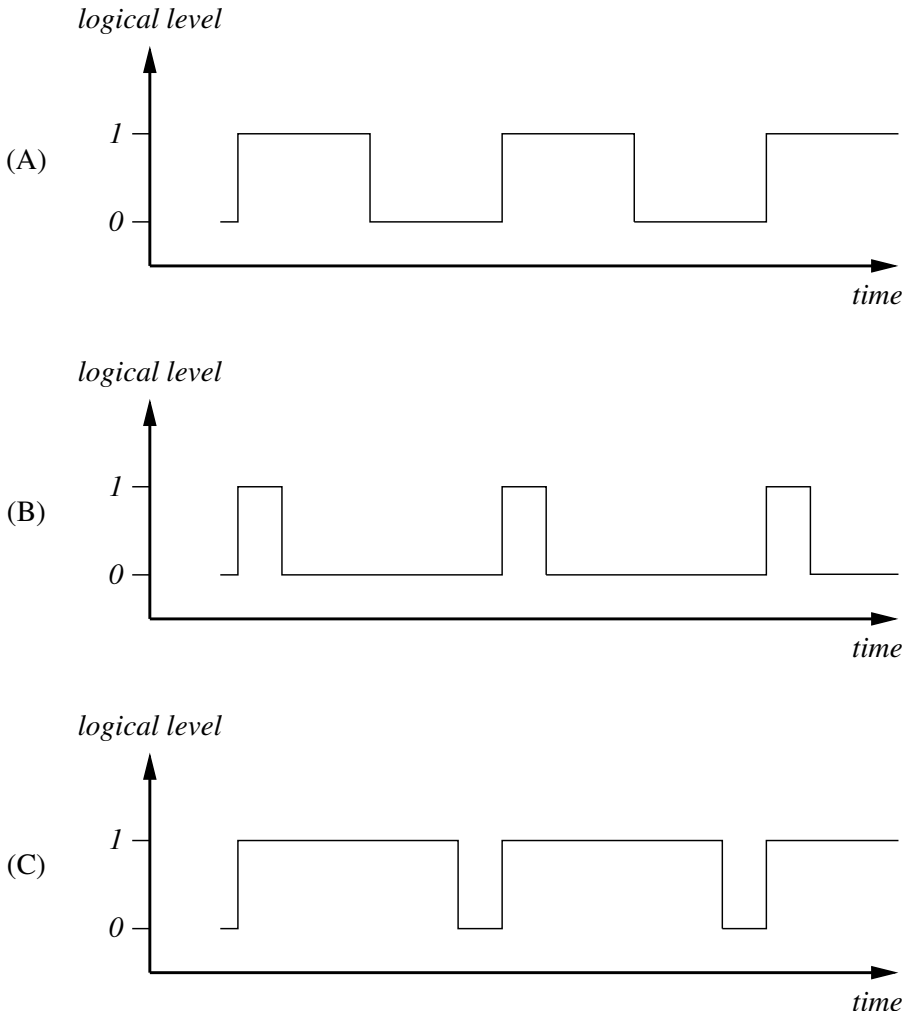

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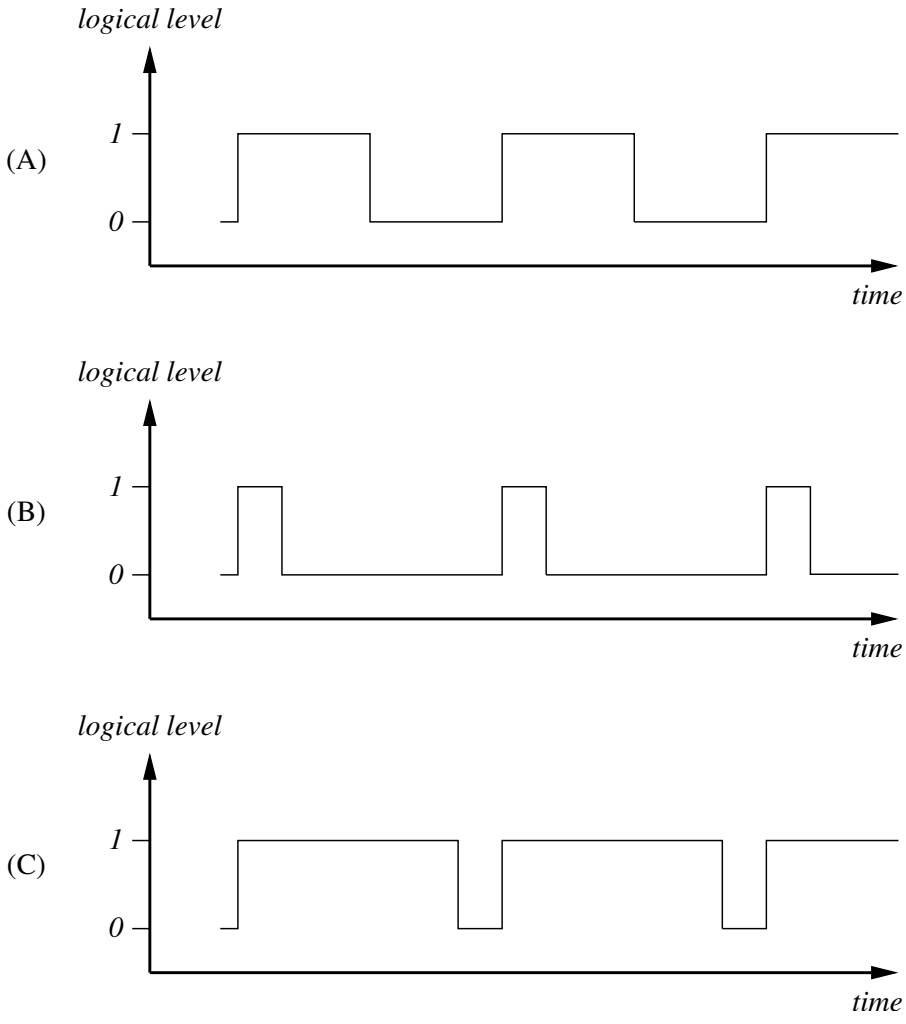

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- We refer to the half-closed interval $[t_i, t_{i+1})$ as clock cycle i.

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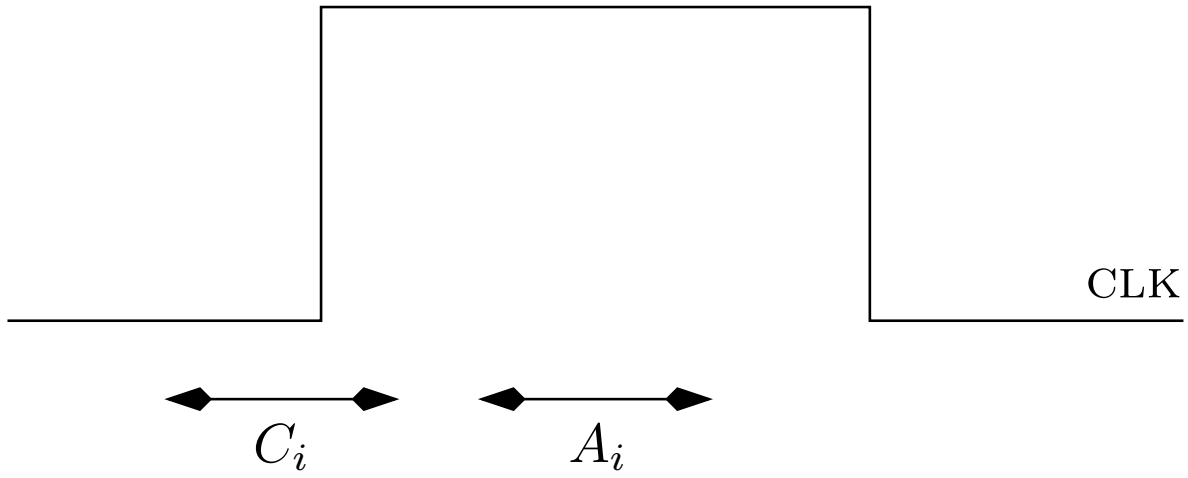

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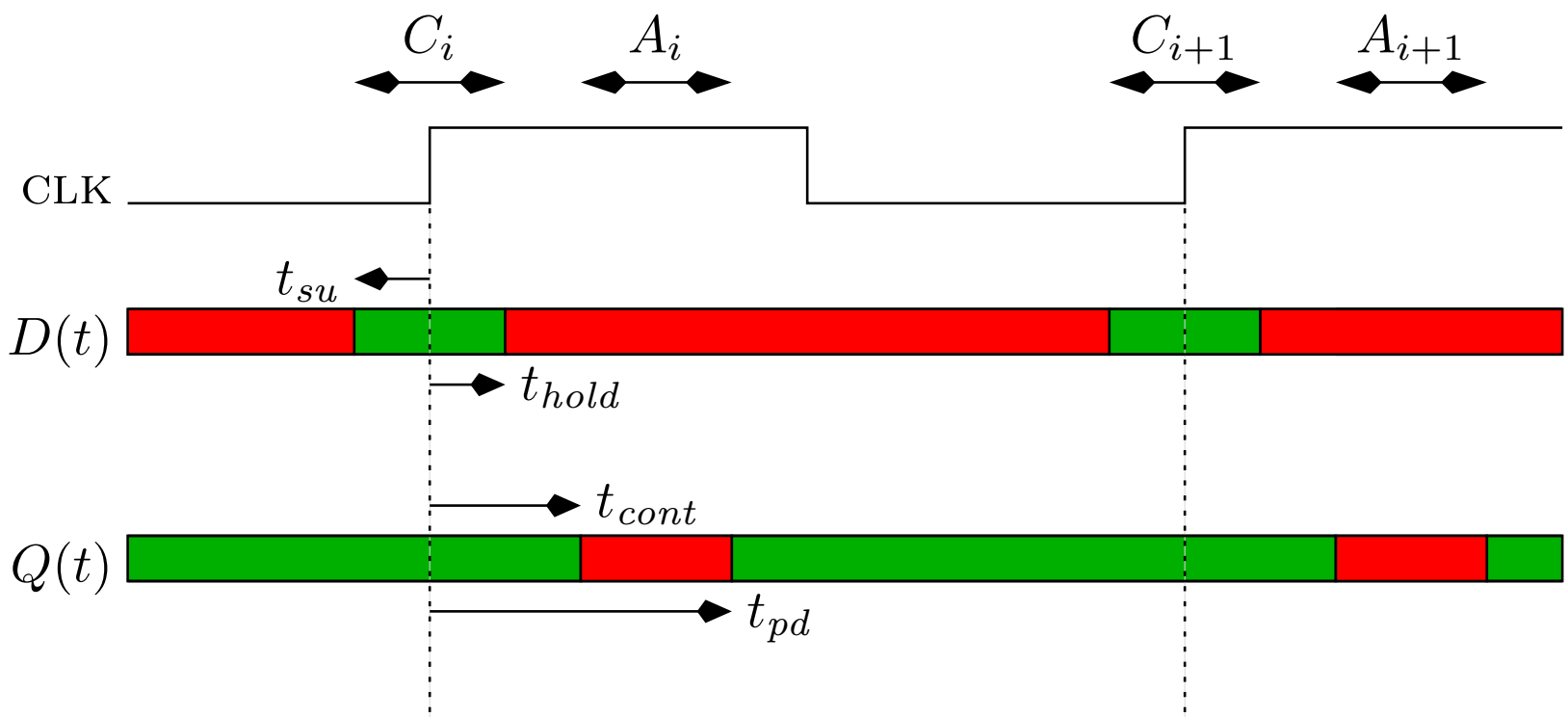
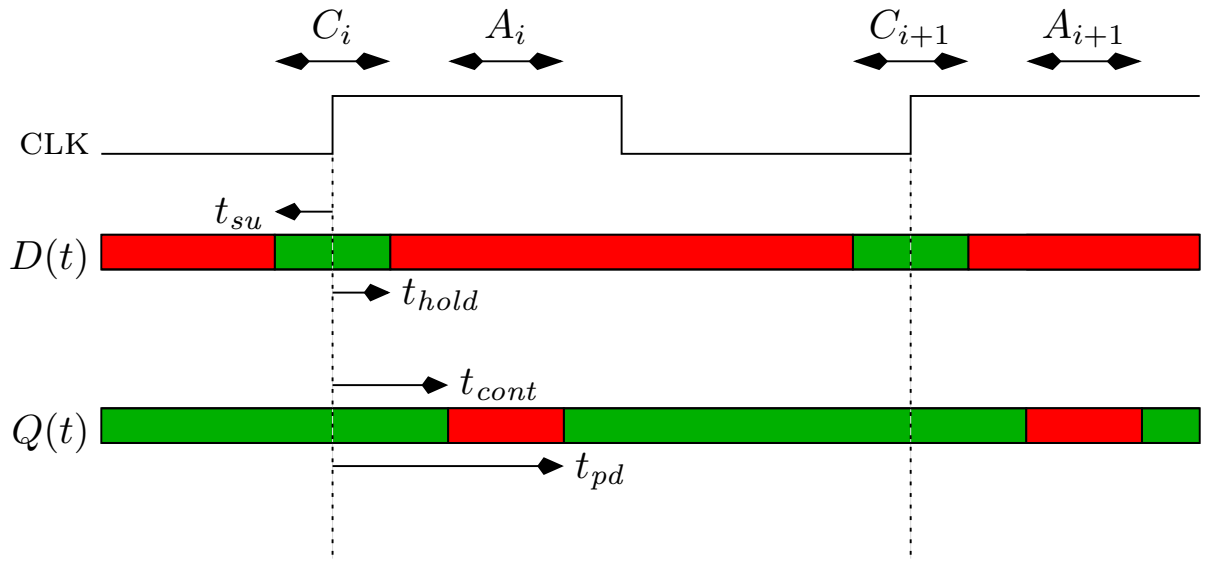


Remarks on definition of flip-flop



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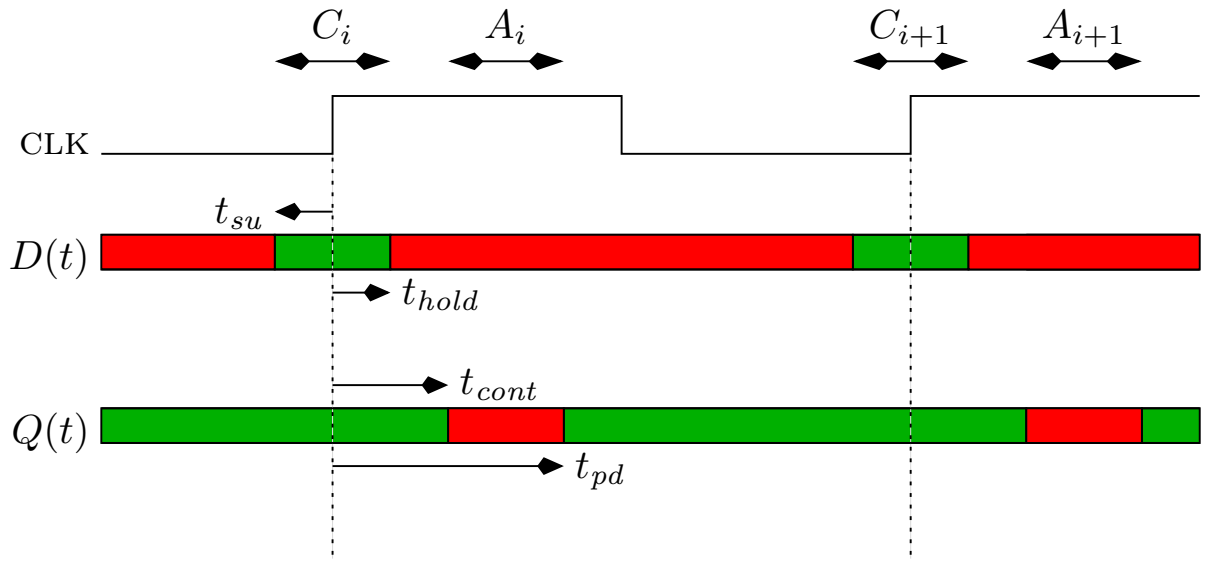

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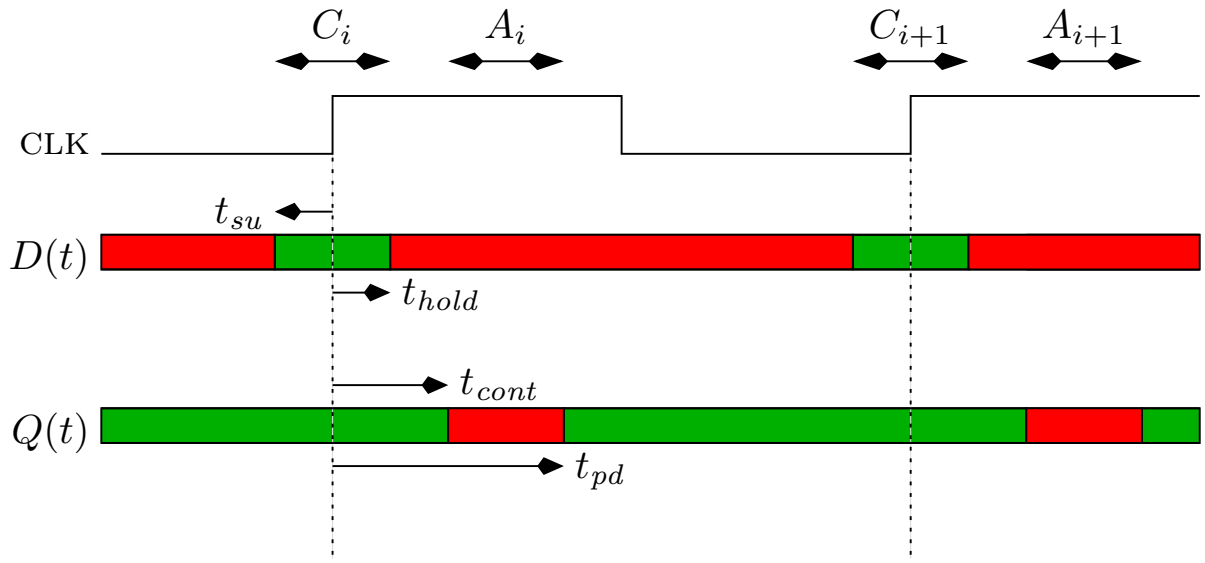

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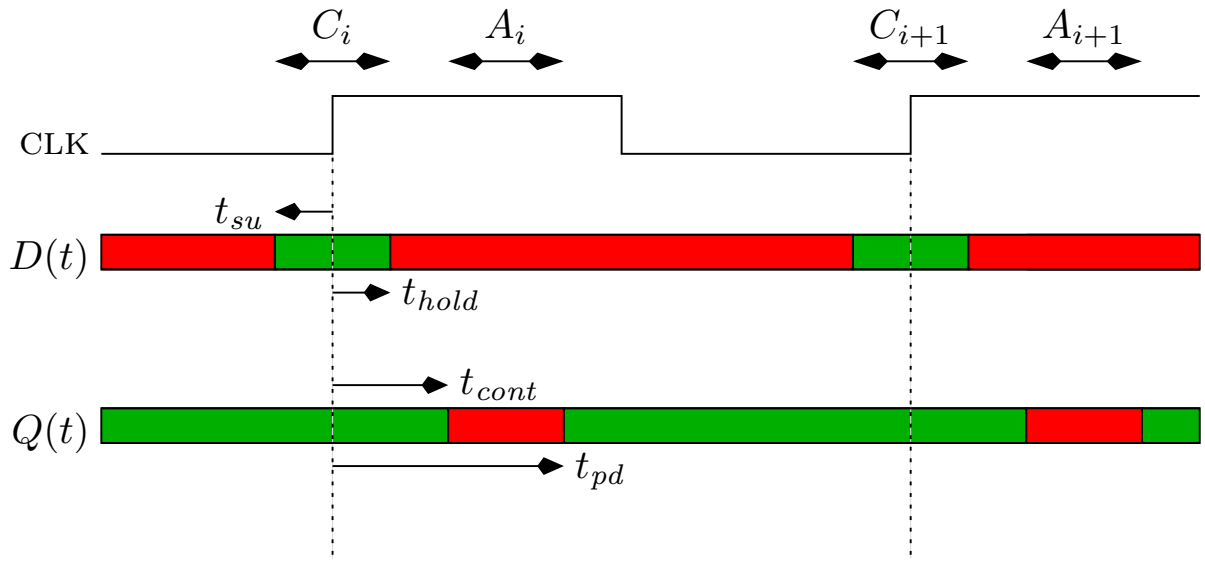

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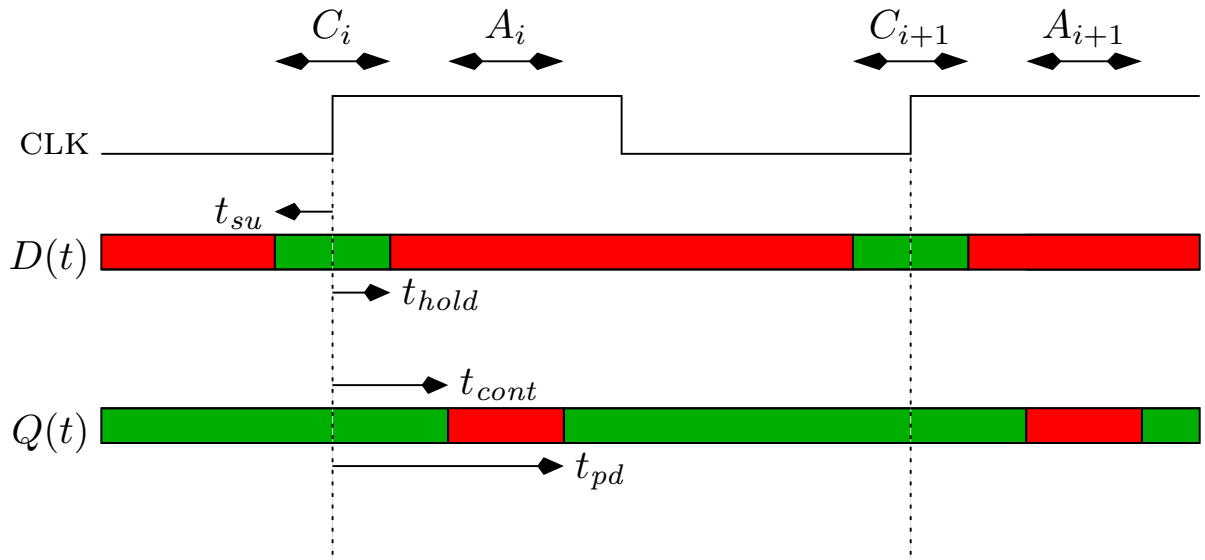

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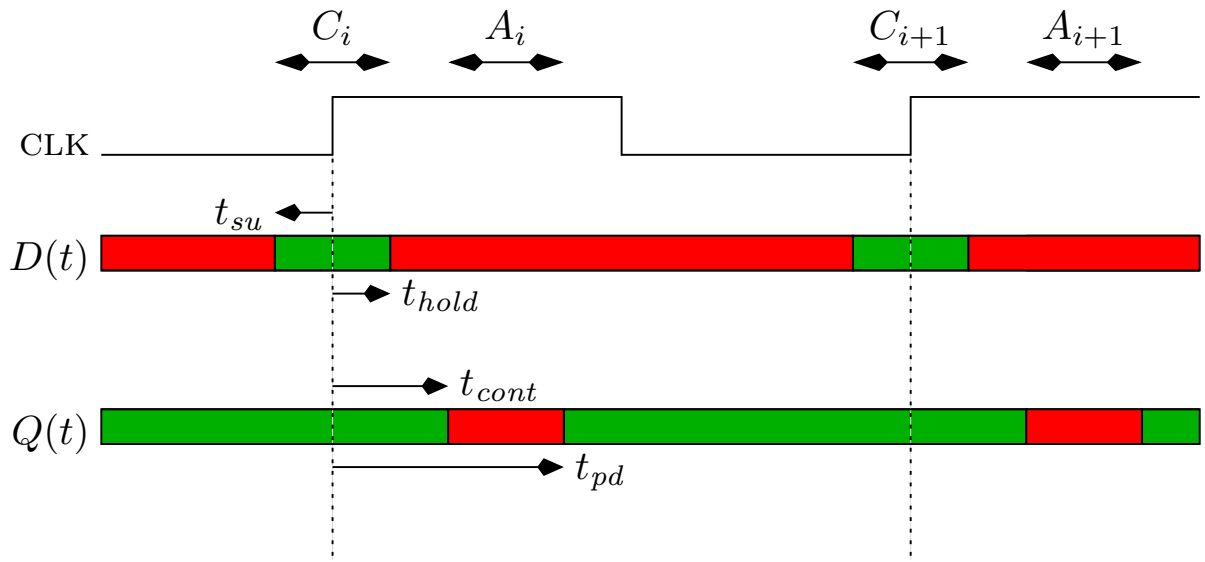
- Flip-flop samples $D(t)$ during C_i. The sampled value $D(t_i)$ is output during the interval $[t_i + t_{pd}, t_{i+1} + t_{cont}]$.
- Sampling is successful only if $D(t)$ is stable while it is sampled. This is why we refer to C_i as a critical segment.

Remarks on definition of flip-flop - cont.



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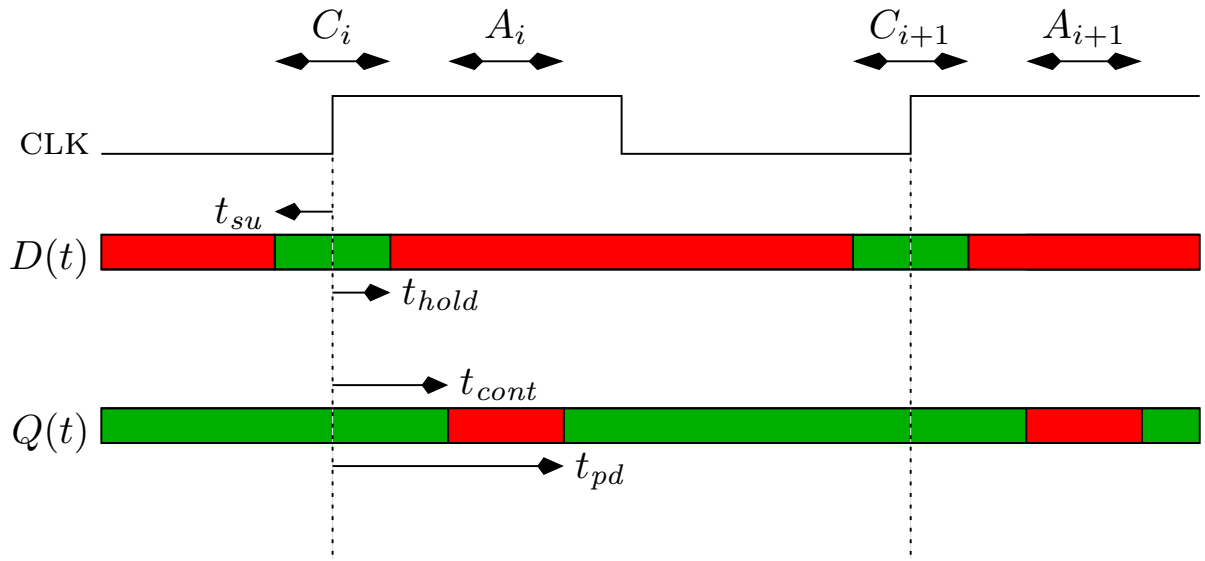

- If the input $D(t)$ is stable during the critical segments $\{C_i\}_i$, then the output $Q(t)$ is stable in between the instability segments $\{A_i\}_i$.

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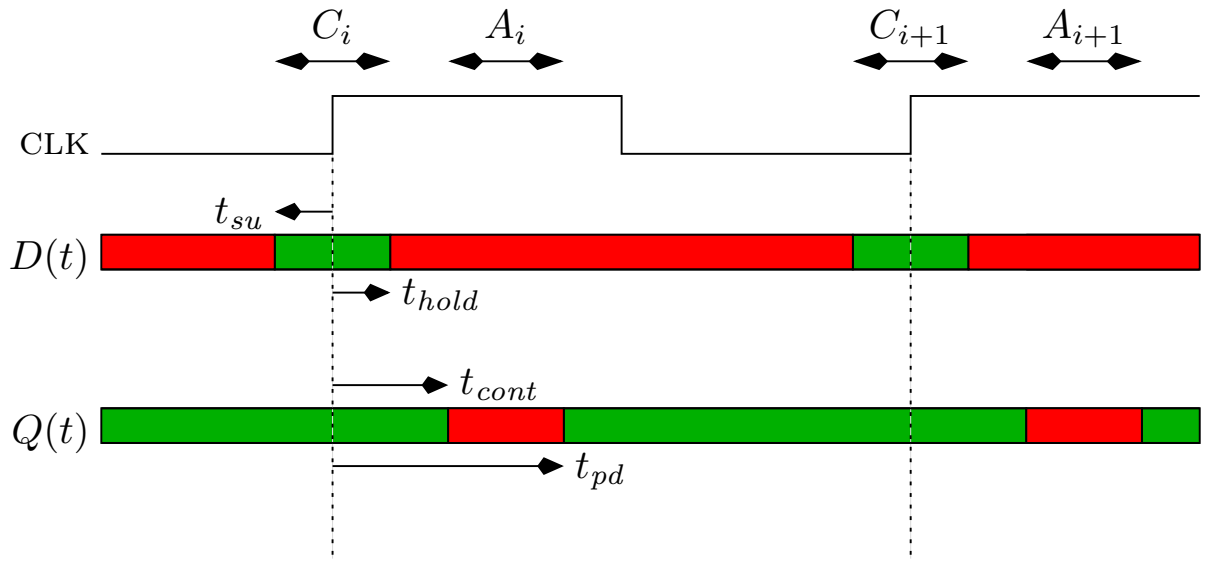

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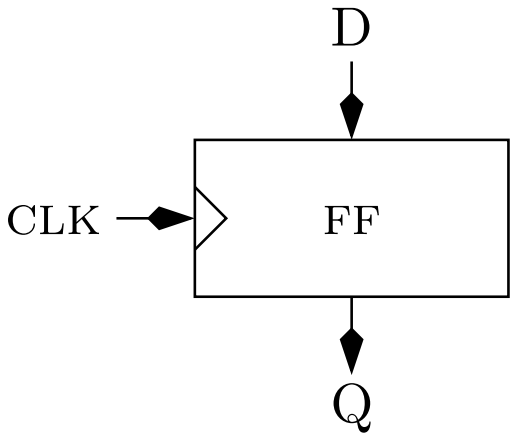
- The stability of the input $D(t)$ during the critical segments depends on the clock period. We will later see that slowing down the clock (i.e. increasing the clock period) helps in achieving a stable $D(t)$ during the critical segments.

schematic of an edge triggered flip-flop



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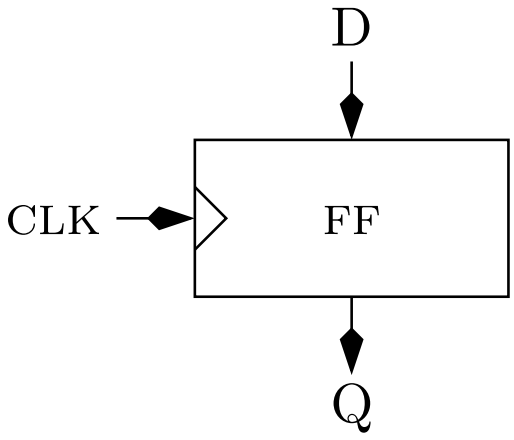

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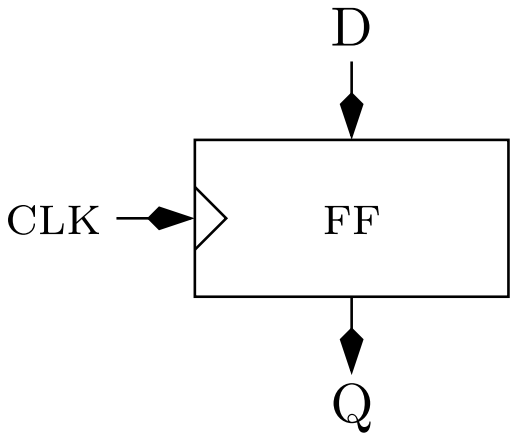

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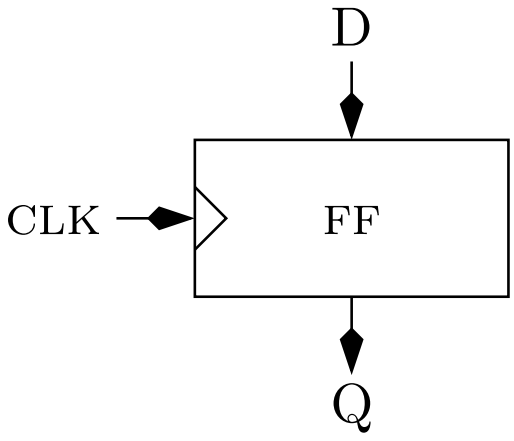

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Question: Prove that an edge-triggered flip-flop is not a combinational circuit.

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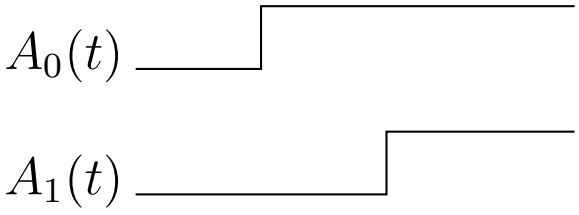
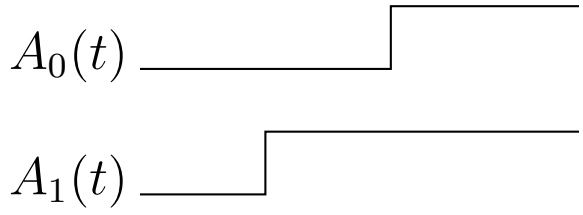
Focus on the task of determining which of two signals reaches 1 first.



$A_0(t)$ reaches 1 first



$A_1(t)$ reaches 1 first

Definition: arbiter

Inputs: Non-decreasing analog signals $A_0(t), A_1(t)$ defined for every $t \geq 0$.

Output: An analog signal $Z(t)$.

Functionality: Assume that $A_0(0) = A_1(0) = 0$. Define T_i, for $i = 0, 1$, as follows:

$$T_i \stackrel{\triangle}{=} \inf\{t \mid \mathit{dig}(A_i(t)) = 1\}.$$

Let $t' \stackrel{\triangle}{=} 10 + \max\{T_0, T_1\}$. The output $Z(t)$ must satisfy, for every $t \geq t'$,

$$\mathit{dig}(Z(t)) = \begin{cases} 0 & \text{if } T_0 < T_1 - 1 \\ 1 & \text{if } T_1 < T_0 - 1 \\ 0 \text{ or } 1 & \text{otherwise.} \end{cases}$$

Arbiter - remarks

$$T_i \stackrel{\triangle}{=} \inf\{t \mid \mathit{dig}(A_i(t)) = 1\}.$$

If T_0 or T_1 equals infinity, then $t' = \infty$, and there is no requirement on the output $Z(t)$.

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- tie: the case that $|T_0 - T_1| \leq 1$.
- In the case of a tie, the arbiter is free to decide, but must decide. $Z(t)$ is stable in the interval $[t, \infty)$.

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- Use the claim to show that flip-flops must have critical segments.

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- Define $A_0(t)$ so that $T_0 = 100$ as follows:

$$A_0(t) \triangleq \begin{cases} \frac{t}{100} \cdot V_{high,in} & \text{if } t \in [0, 100] \\ V_{high,in} & \text{if } t > 100. \end{cases}$$

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- Fix a parameter $x \in [-2, 2]$ and define $A_1(t)$ so that $T_1 = 100 + x$ as follows:

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- Define the function $f(x)$ by $f(x) \triangleq Z(200)$.

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$$A_0(t) \triangleq \begin{cases} \frac{t}{100} \cdot V_{high,in} & \text{if } t \in [0, 100] \\ V_{high,in} & \text{if } t > 100. \end{cases}$$

- Fix a parameter $x \in [-2, 2]$ and define $A_1(t)$ so that $T_1 = 100 + x$ as follows:

$$A_1(t) \triangleq \begin{cases} \frac{t}{100+x} \cdot V_{high,in} & \text{if } t \in [0, 100 + x] \\ V_{high,in} & \text{if } t > 100 + x. \end{cases}$$

- Define the function $f(x)$ by $f(x) \triangleq Z(200)$.
- We study the function $f(x)$ in the interval $x \in [-2, 2]$.

Proof: every circuit C is not an arbiter - cont.

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- $x = 2 \Rightarrow T_1 = 100 + x = 102$. It follows that $A_0(t)$ "wins", and *dig*$(Z(200)) = 0$. Hence $f(2) \leq V_{\mathit{low,out}}$.

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Proof: $f(x)$ is continuous - cont.

- Consider an infinitesimal change in x. This change affects $A_1(t)$ but does not affect $A_0(t)$ and the initial state.

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- $\Rightarrow f(x)$ is continuous.

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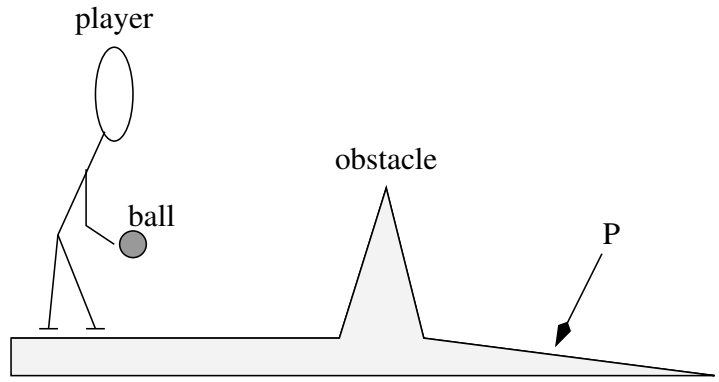
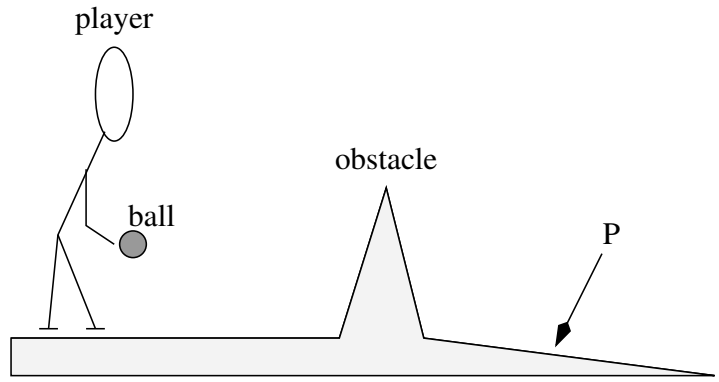
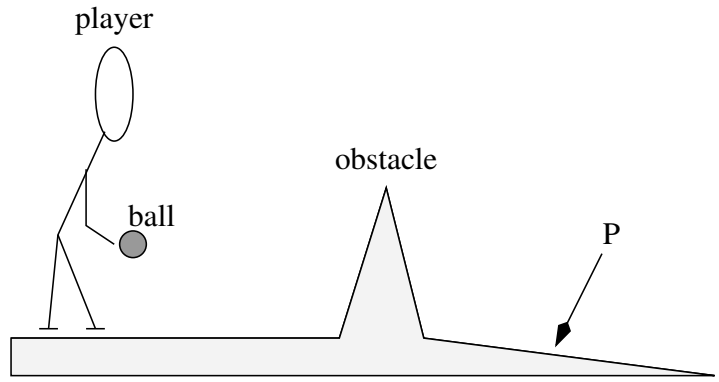
  2. we allow the judge several hours to decide.
  3. we allow the judge to decide arbitrarily if the running times of the winner and runner-up are within a second.


player
obstacle
ball
P



- Player - rolls a ball. Judge - announces decision if ball passes point P one day after.



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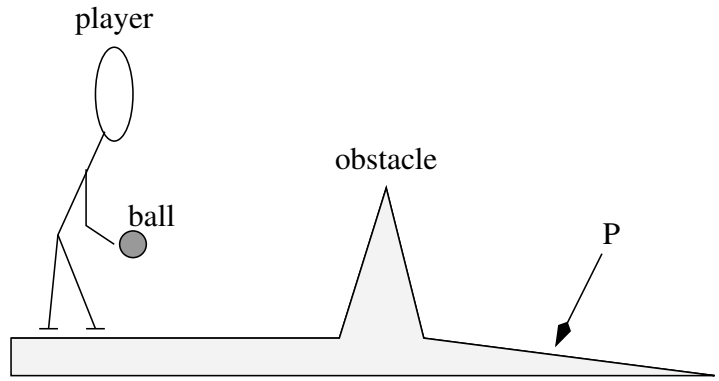

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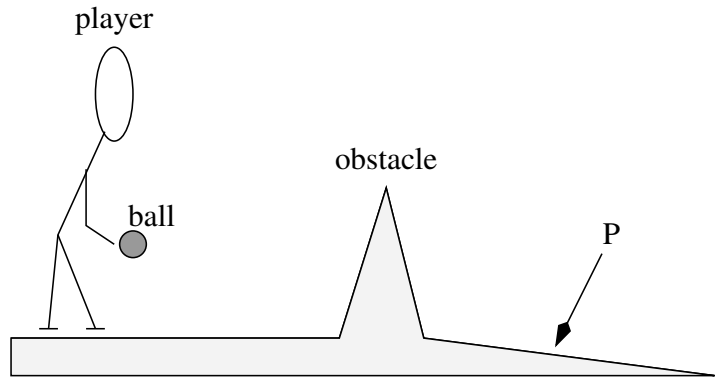

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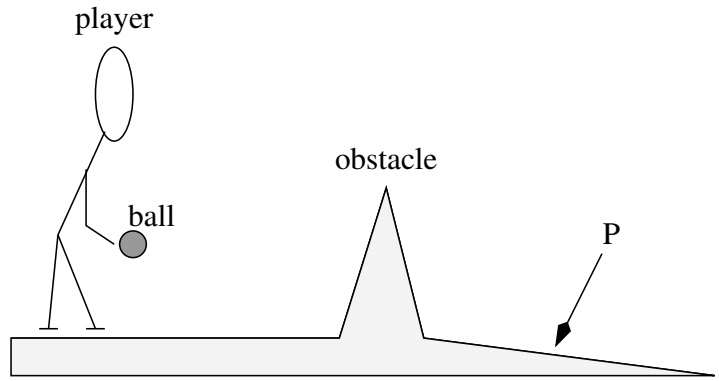

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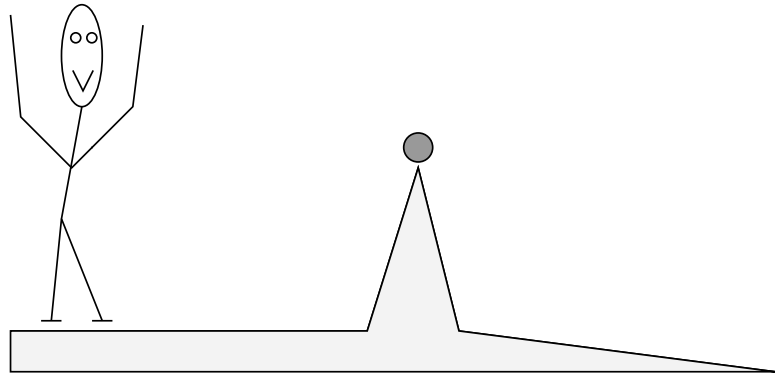
Judge is in trouble:

- If speed$= v'$, then the ball reaches the tip of the obstacle and may remain there indefinitely long!
- If the ball remains on the obstacle's tip 24 hours past the throw, then the judge cannot announce her decision.

Meta-stability



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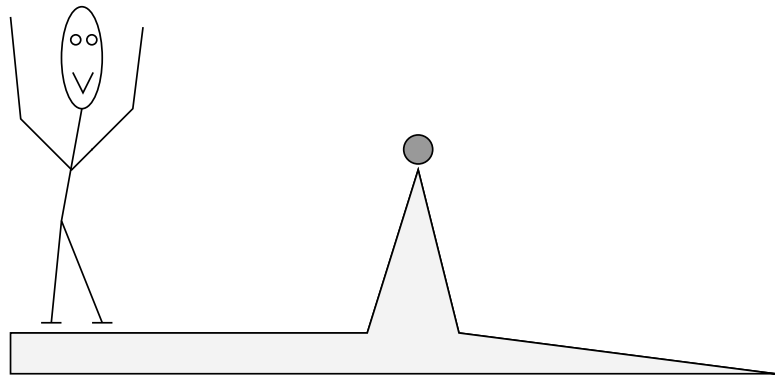

- Meta-stability - a state of equilibrium (i.e. zero force) which is not a local minimum of energy (i.e. a slight force causes a movement away from the state).

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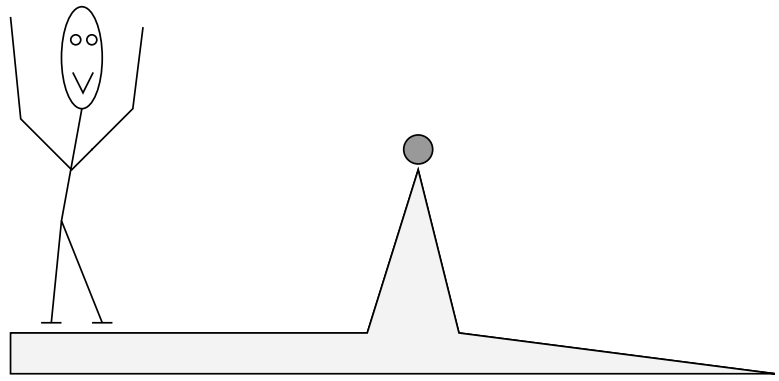

- Meta-stability - a state of equilibrium (i.e. zero force) which is not a local minimum of energy (i.e. a slight force causes a movement away from the state).
- Inclined to say that the "probability of meta-stability occurring is very small". This requires a probability distribution over the rolling speed v where

$$\lim_{\varepsilon \to 0} \mathit{Pr}(|v - v'| < \varepsilon) = 0.$$

Lessons learned

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- Certain tasks are not achievable with probability 1.
  - coin toss might end up with the coin standing on its perimeter.
  - noise could be big enough to cause the digital value of a signal to flip from zero to one. (increase noise margin to reduce the probability of such an event.)

Reducing the probability of meta-stability

- Increase length of segment of instability. Increasing the delay of the arbiter (significantly) decreases the chances of meta-stability. E.g., ball resting on the tip of the obstacle is likely to fall to one of the sides.

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- Increase the slope of the transfer function in the range of non-logical values. Similar to sharpening the tip of the obstacle.
- However, increasing the clock rate means that "decisions" must be made faster (i.e. within a clock period) and the chance of meta-stability increases.

Question

Does the proof of the Claim hold only if the signals $A_i(t)$ rise gradually?

Question: Prove the claim with respect to "fast" non-decreasing signals $A_i(t)$. Namely, the length of the interval during which *dig*$(A_i(t))$ is non-logical equals ε.

Flip-flops: necessity of critical segments

DEF: A flip-flop without a critical segment is a flip-flop in which the setup-time and hold-time satisfy $t_{su} = t_{hold} = 0$. The functionality is defined as follows:

- For every i, $Q(t)$ is logical (either zero or one) during the interval $t \in (t_i + t_{pd}, t_{i+1} + t_{cont})$ regardless of whether $D(t_i)$ is logical.
- If $D(t_i)$ is logical, then $Q(t) = D(t_i)$ during the interval $t \in (t_i + t_{pd}, t_{i+1} + t_{cont})$.

Flip-flops: necessity of critical segments

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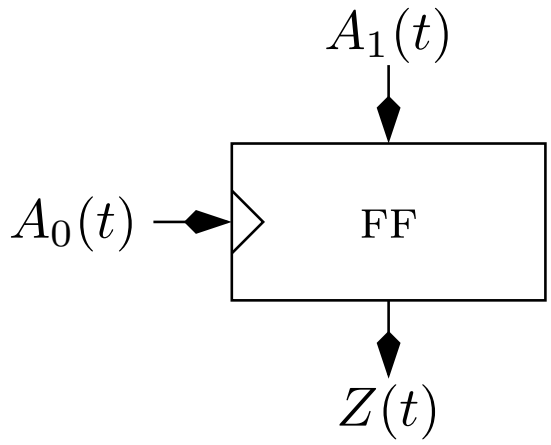
- If $D(t_i)$ is logical, then $Q(t) = D(t_i)$ during the interval $t \in (t_i + t_{pd}, t_{i+1} + t_{cont})$.

Just as the arbiter's decision is free if a tie occurs, the flip-flop is allowed to output either zero or one if $D(t_i)$ is not logical. However, the output of the flip-flip must be logical once the instability segment ends.

An arbiter based on a flip-flop without a critical segment



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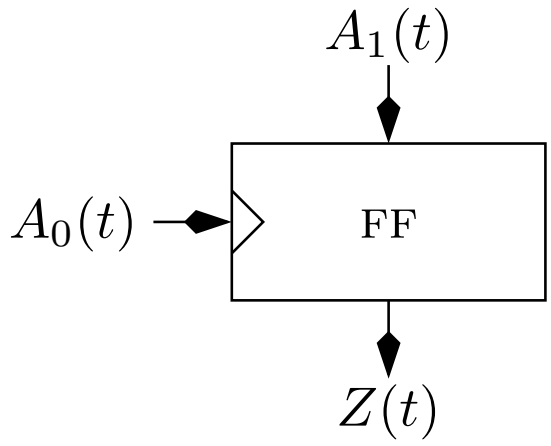

Assumptions:

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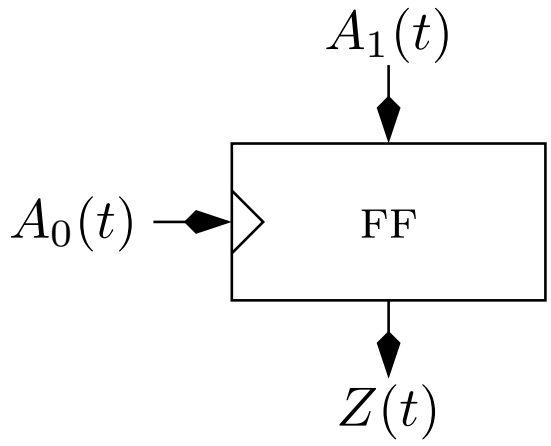

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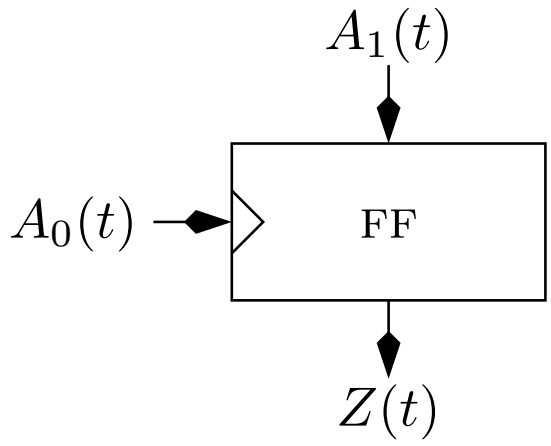

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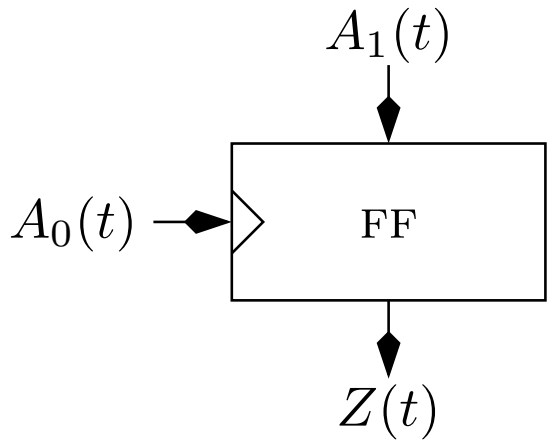

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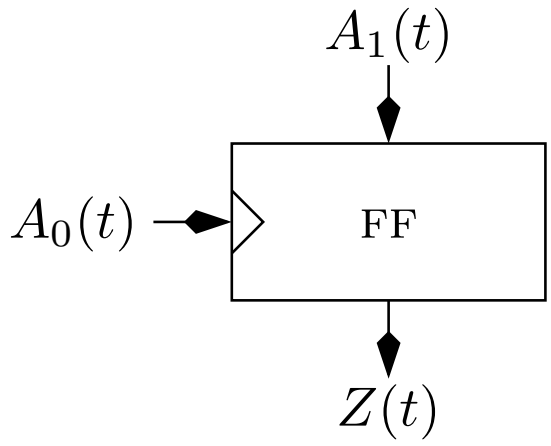

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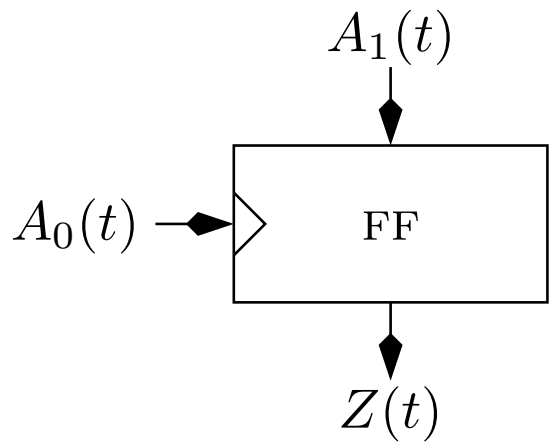

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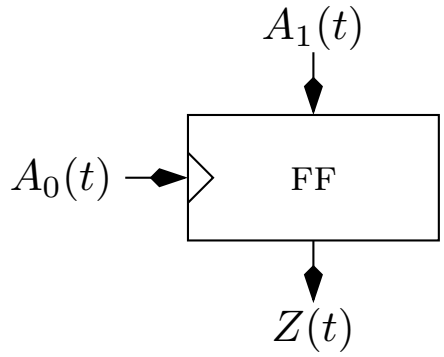
CORO: There does not exist a flip-flop without a critical section.

Remarks



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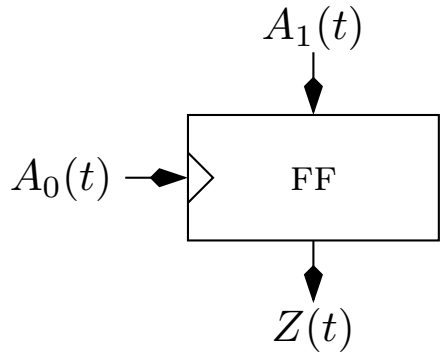

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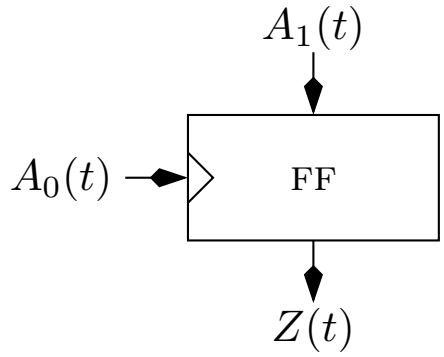

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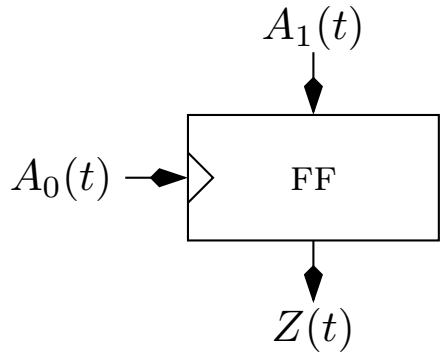

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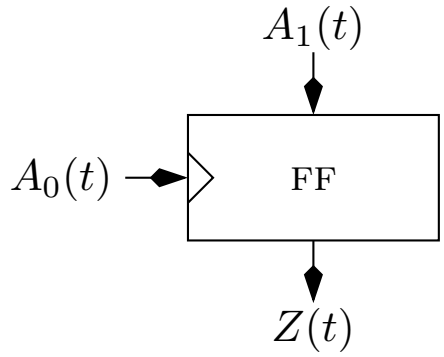

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- the claim assumes only one “tick of the clock”, so we may regard $A_0(t)$ as a clock with a very long period.
- proof of claim does not rely on $A_0(t)$ rising slowly; the claim holds regardless of the rate of change of $A_0(t)$.

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- $T_1 < T_0 - 1$: if $T_1 < T_0 - 1$, then *dig*$(A_1(T_0)) = 1$. Hence sampled value equals 1, and hence, *dig*$(Z(t)) = 1$, for every $t \geq T_0 + t_{pd}$.

Proof that circuit is an arbiter

We consider three cases:

- $|T_1 - T_0| \leq 1$: flip-flop's output $Z(t)$ is always logical at time $T_0 + t_{pd}$, so circuit functions properly.
- $T_1 < T_0 - 1$: if $T_1 < T_0 - 1$, then $dig(A_1(T_0)) = 1$. Hence sampled value equals 1, and hence, $dig(Z(t)) = 1$, for every $t \geq T_0 + t_{pd}$.
- $T_0 < T_1 - 1$: we claim that $dig(A_1(T_0)) = 0$, and hence, $dig(Z(t)) = 0$, for every $t \geq T_0 + t_{pd}$.

Proof that circuit is an arbiter - cont.

We need to show that $T_0 < T_1 - 1 \Rightarrow dig(A_1(T_0)) = 0$.

Proof that circuit is an arbiter - cont.

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- $T_0 < T_1 \Rightarrow$ *dig*$(A_1(T_0)) \in \{0,$ non-logical$\}$.

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Hence, $T_1 \leq T_0 + 10^{-9}$ contradicting $T_1 > T_0 + 1$.

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It follows that if $T_0 < T_1 - 1$, then *dig*$(A_1(T_0)) = 0$. QED

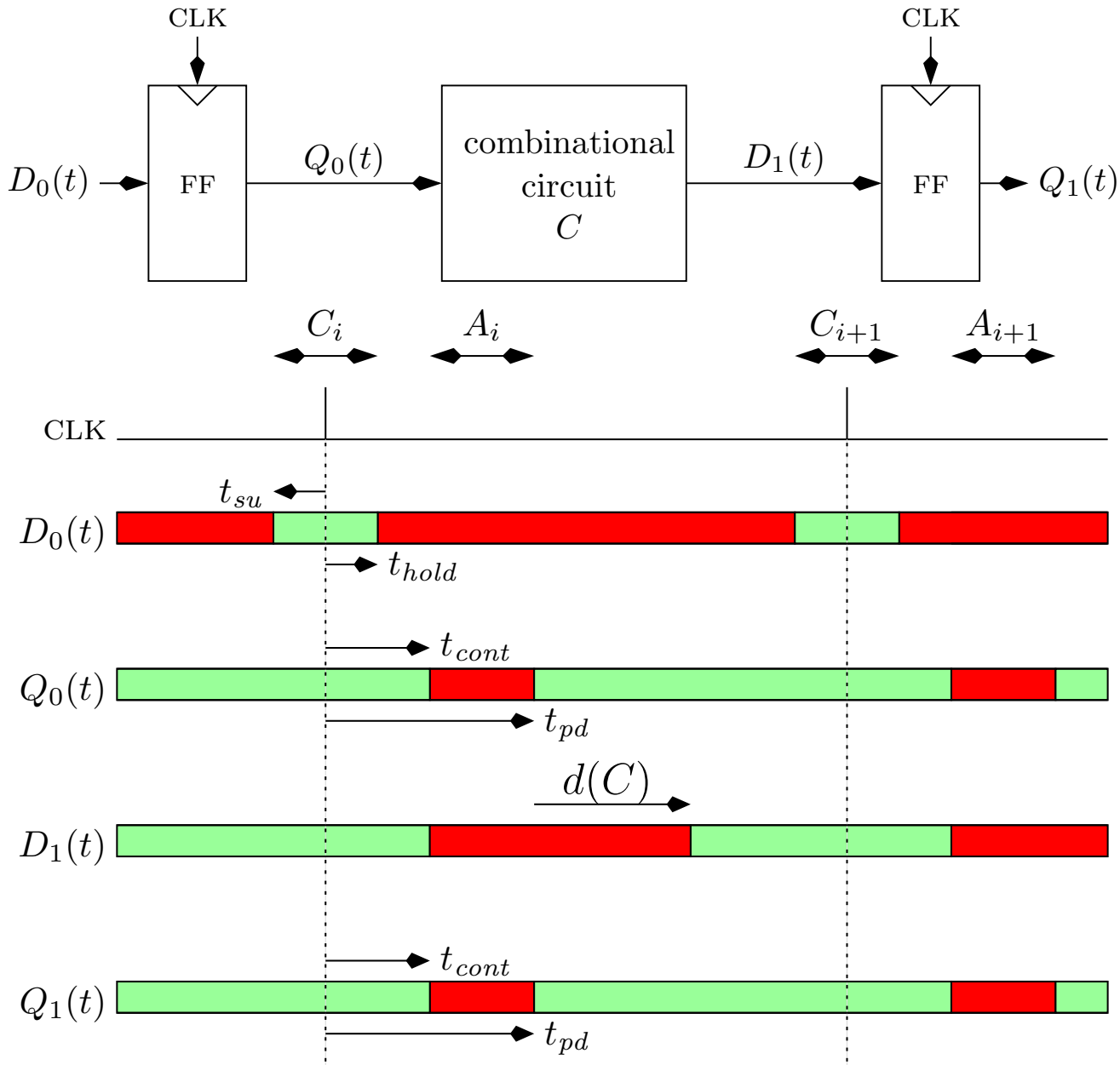
Corollary: conclusion

Critical segment is required to avoid meta-stability of the flip-flop.

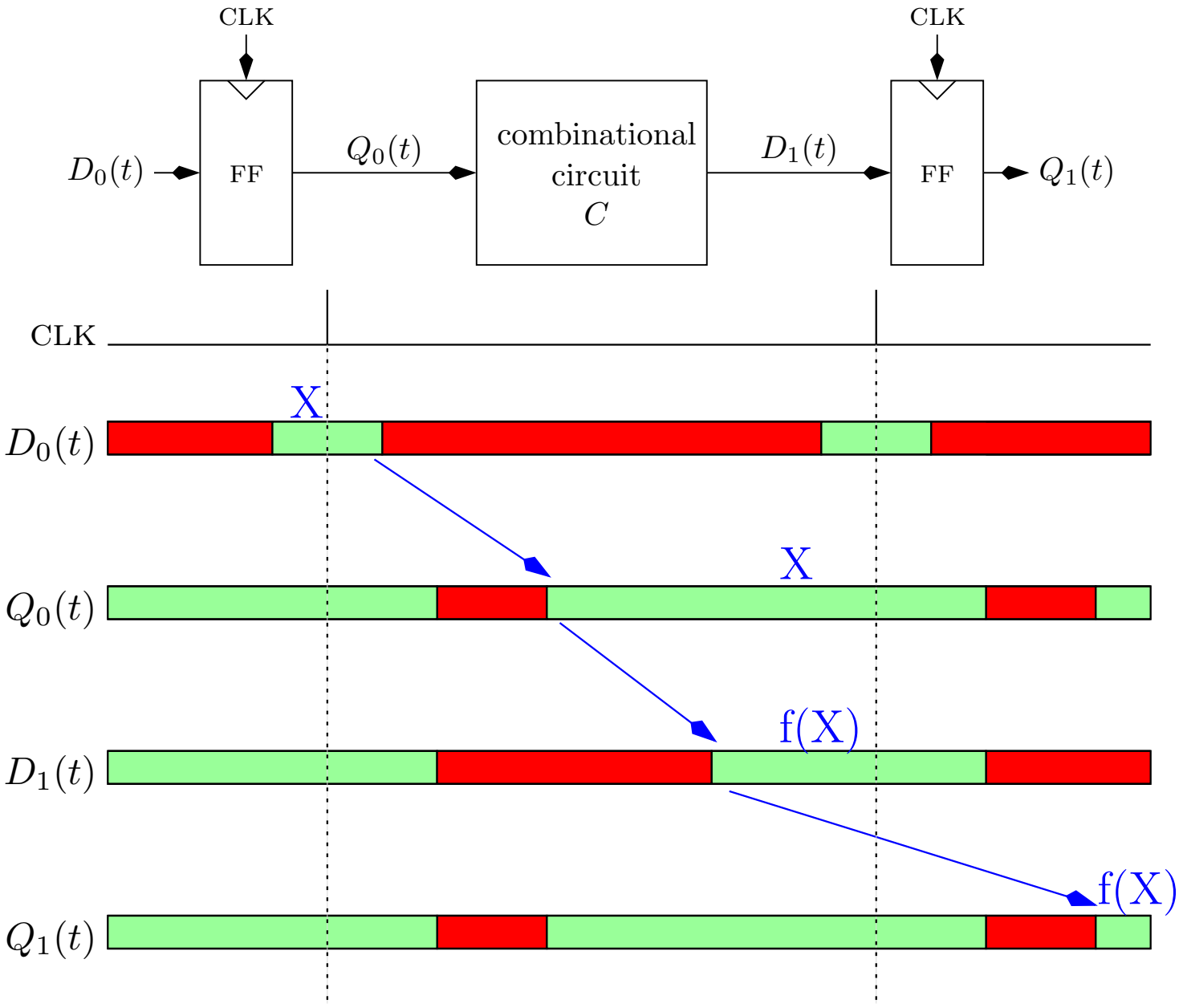
Without critical segment, flip-flop's output can be non-logical

even after $t_i + t_{pd}$.

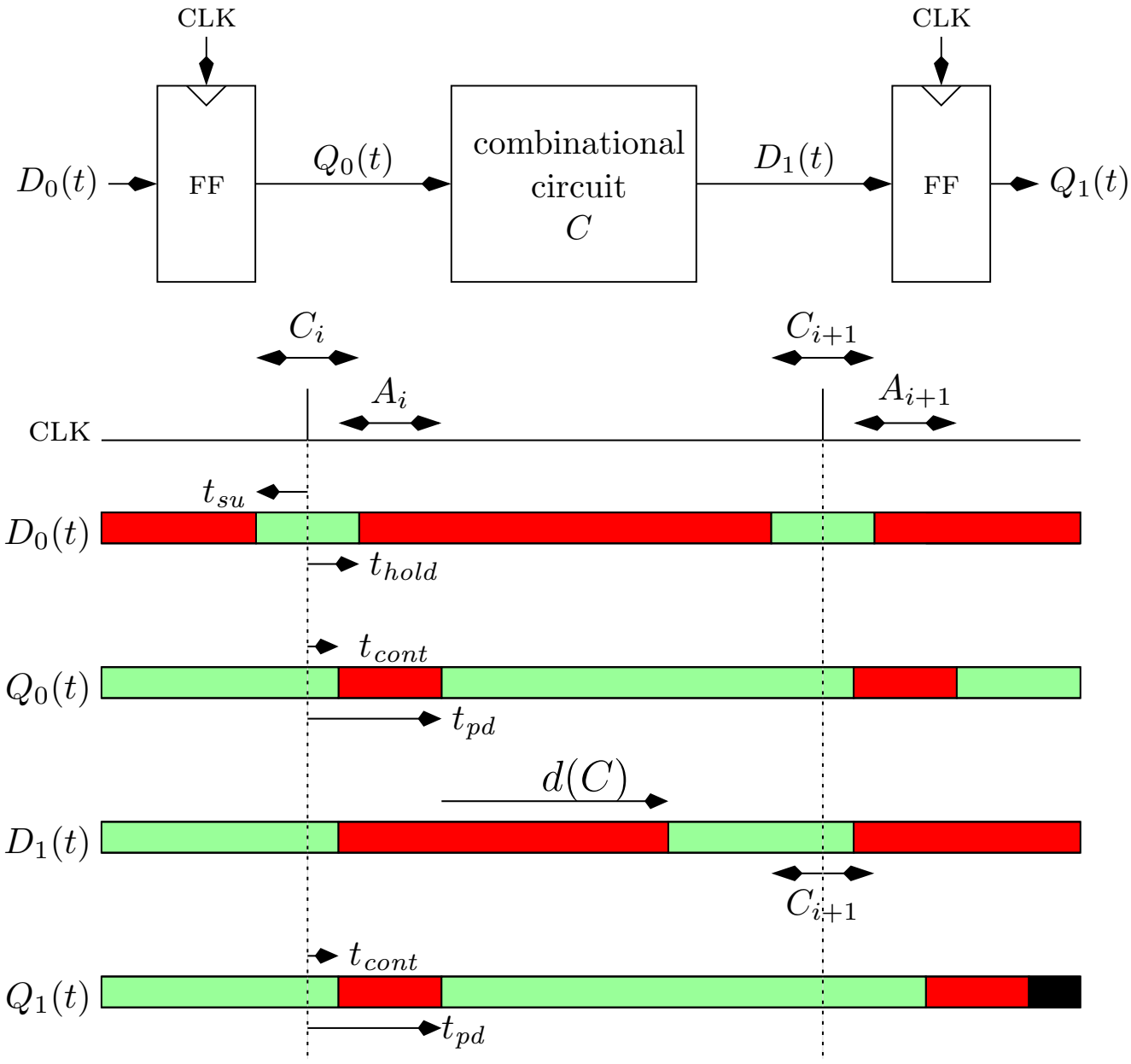
An example: timing



An example: functionality



Non-disjoint segments: $A_i \cap C_i \neq \emptyset$



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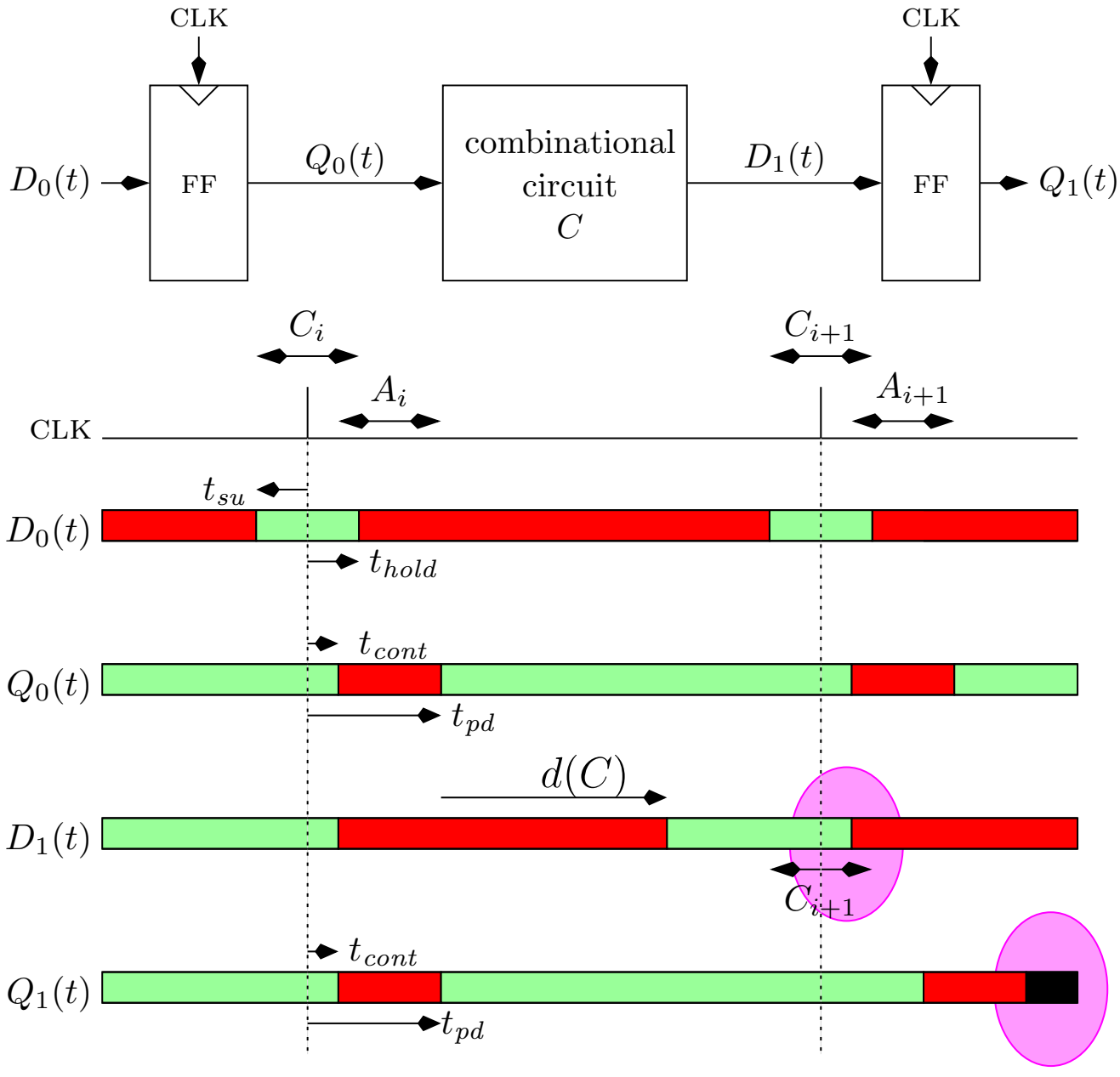

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If $t_{cont} + cont(C) > t_{hold}$, then the signal $D_1(t)$ is stable during the critical segment C_{i+1}, and correct functionality is obtained.

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- Relying on the contamination delay of combinational circuits complicates timing analysis.
- We use a strict assumption that *cont*$(C) = 0$, for every combinational circuit C. This does not cause incorrect circuits even if *cont*$(C) > 0$.

Fixing $A_i \cap C_i \neq \emptyset$

Question: Assume that we have an edge-triggered flip-flop FF in which $t_{hold} > t_{cont}$. Suppose that we have an inverter with a contamination delay $cont(\mathsf{INV}) > 0$.

- Suggest how to design an edge-triggered flip-flop FF′ that satisfies $t_{hold}(\mathsf{FF}') < t_{cont}(\mathsf{FF}')$.
- What are the parameters of FF′?

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- d - combinational delay of the D-latch.

D-Latch: definition

- During the interval $[t_i + d, t'_i)$, the output $Q(t)$ satisfies: $Q(t) = D(t)$, provided that $D(t)$ is stable during the interval $[t - d, t]$. We say that the D-latch is transparent during the interval $[t_i + d, t'_i)$.

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- During the interval $(t'_i + t_{hold}, t_{i+1})$, if $D(t)$ is stable during the critical segment $[t'_i - t_{su}, t'_i + t_{hold}]$, then $Q(t) = D(t'_i)$. We say that the D-latch is opaque during the interval $(t'_i + t_{hold}, t_{i+1})$.

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- using D-latches wisely leads to faster designs.
- designs based on D-latches require multiple clock phases (or at least a clock CLK and its negation $\overline{\text{CLK}}$).
- Although timing with multiple clock phases is an important and interesting topic, we do not deal with it in this course.

Definition : clock enabled flip-flips

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Inputs: Digital signals $D(t), \mathsf{CE}(t)$ and a clock CLK.

Output: A digital signal $Q(t)$.

Functionality: If $D(t)$ and $\mathsf{CE}(t)$ are stable during the critical segment C_i, then for every $t \in (t_i + t_{pd}, t_{i+1} + t_{cont})$

$$Q(t) = \begin{cases} D(t_i) & \text{if } \mathsf{CE}(t_i) = 1 \\ Q(t_i) & \text{if } \mathsf{CE}(t_i) = 0. \end{cases}$$

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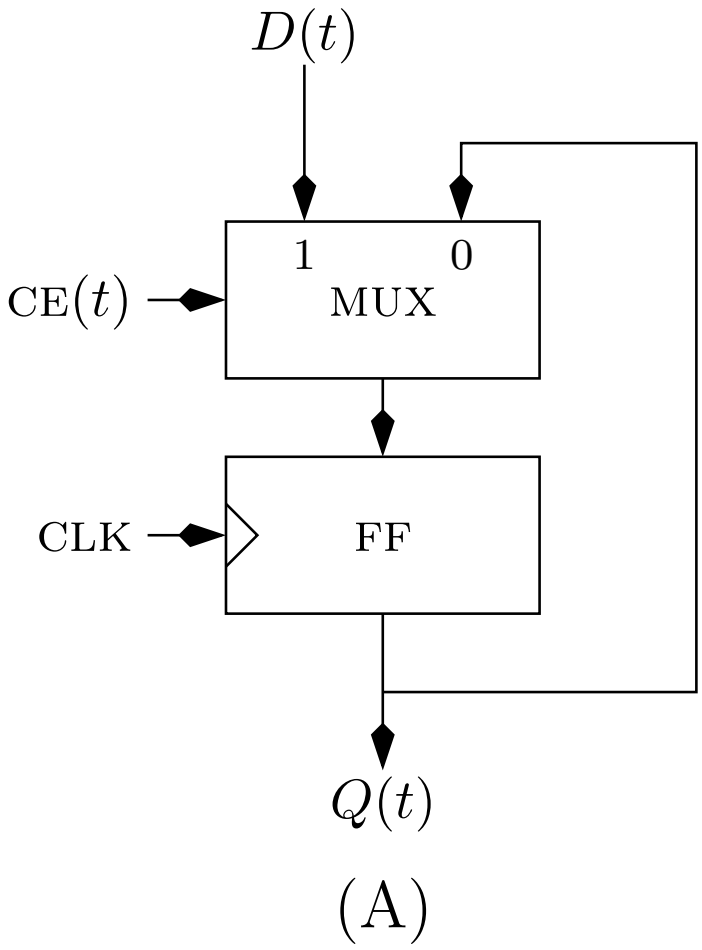
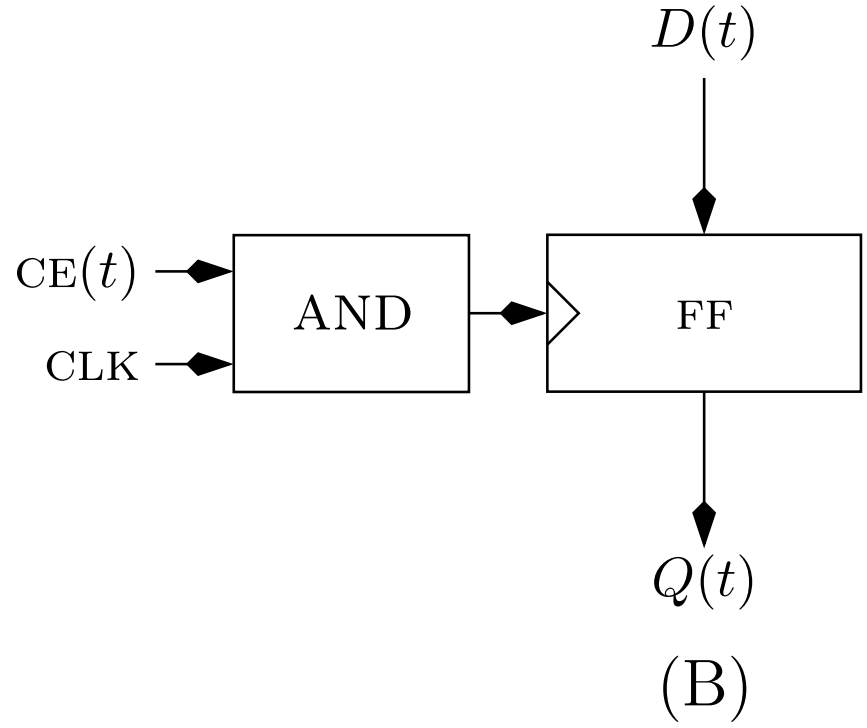
- $\mathsf{CE}(t)$ - clock-enable signal.
- $\mathsf{CE}(t)$ indicates whether the flip-flop samples the input $D(t)$ or maintains its previous value.

Clock enabled flip-flips : implementation

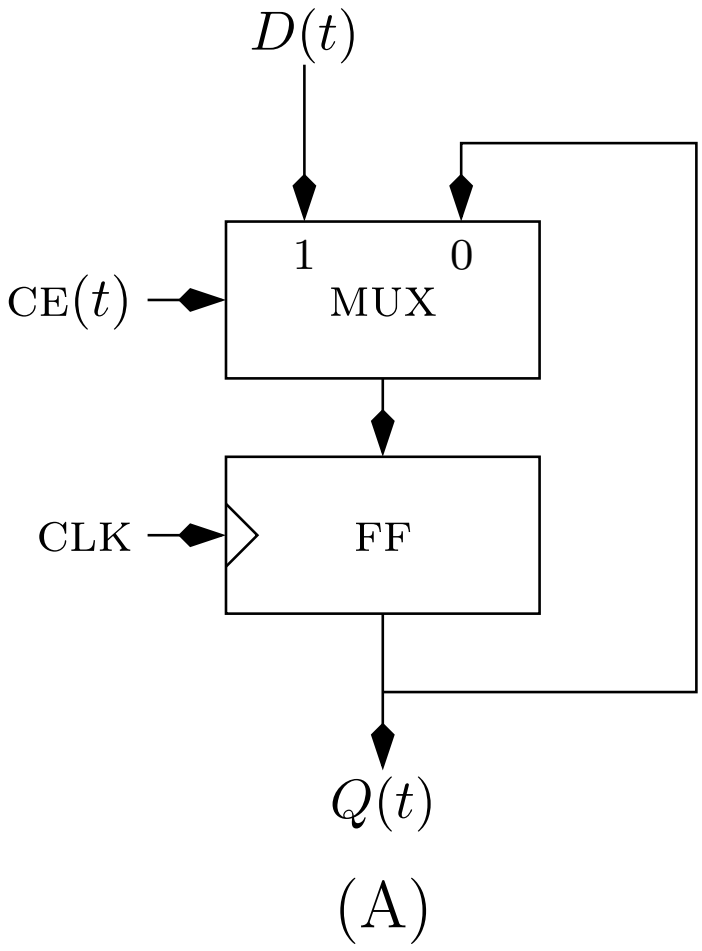


(A)



(B)

Clock enabled flip-flips : implementation



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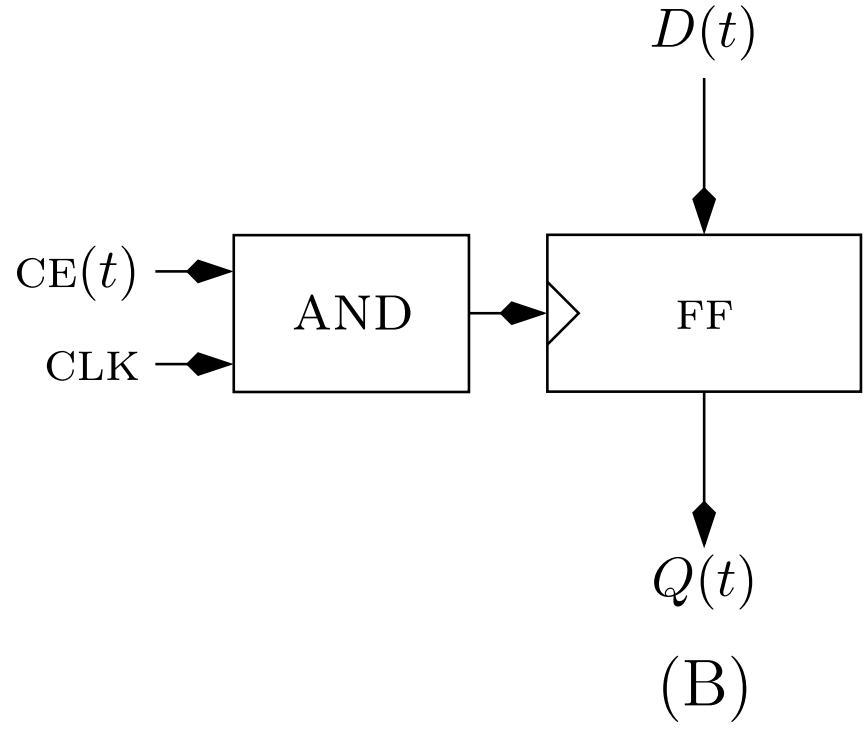
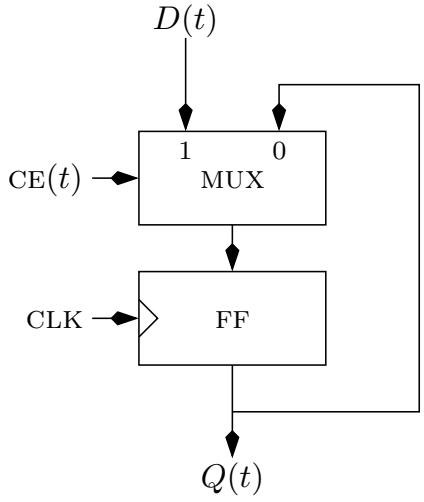


(B)

Question: Which design is correct?

Clock enabled flip-flips : implementation - cont



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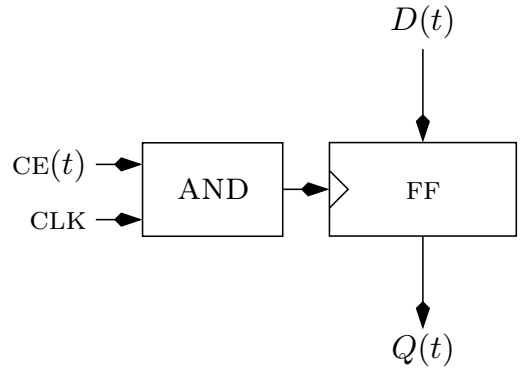

(B)

Design (B) is wrong because:

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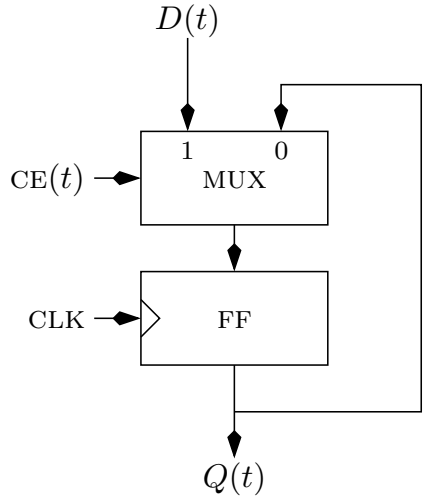

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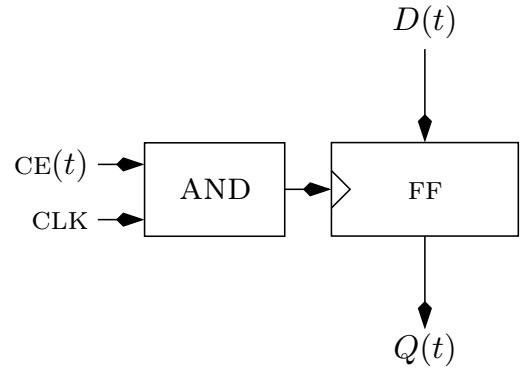

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- output of the AND-gate is not a clock signal (glitches).

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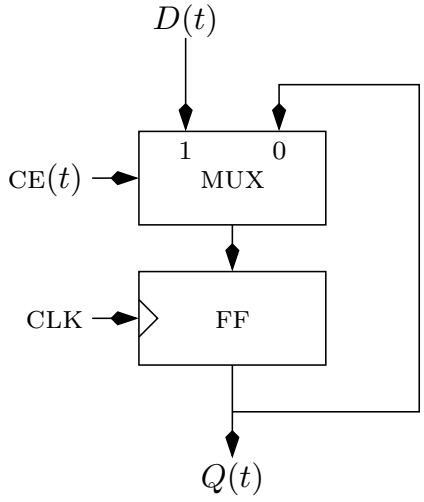

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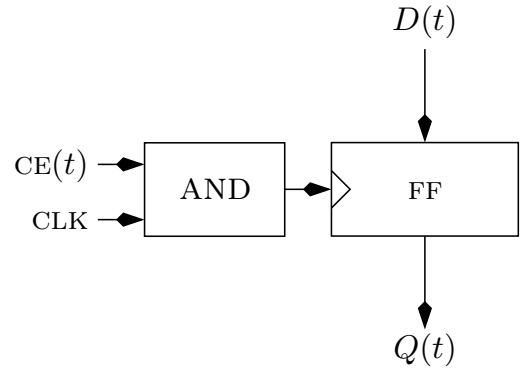

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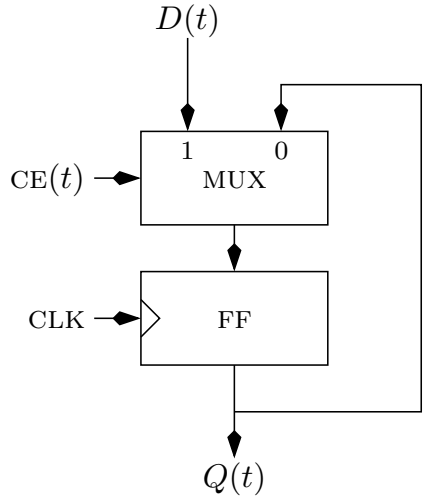

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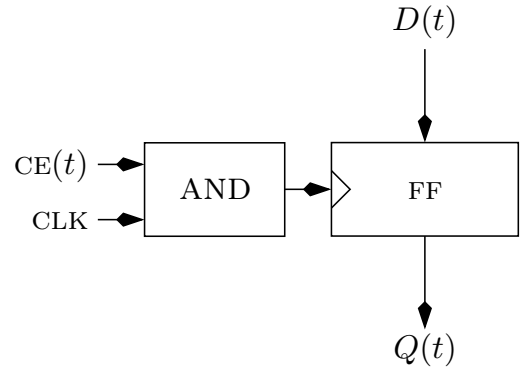

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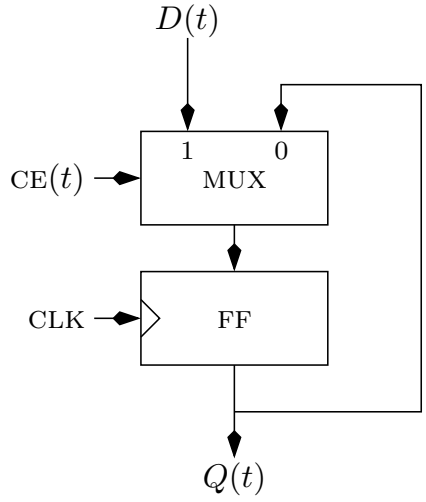
- output of the AND-gate is not a clock signal (glitches).
- slow transitions of the output of the AND-gate (increase hold time)
- in some technologies, the flip-flop does not retain the stored bit forever. $\Rightarrow$ if $\mathrm{CE}(t) = 0$ for a long period, then the flip-flop's output may become non-logical.

Clock enabled flip-flips : implementation - cont



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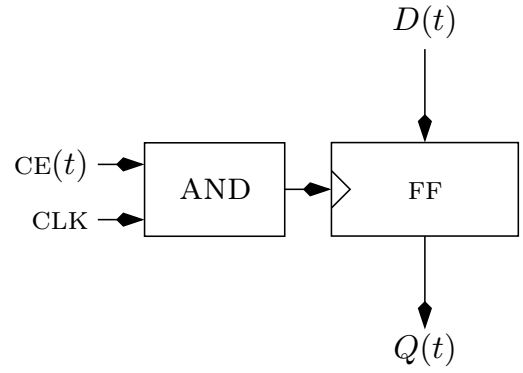

(B)

Question: Compute the parameters of the clock-enabled flip-flop depicted in part (A) in terms of the parameters of the edge-triggered flip-flop and the MUX.

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- other memory devices: D-latch & clock-enabled flip-flop