1. Consider a combinational circuit *Partial_Sums*(n, m) defined as follows:

   - Inputs: $a_1[n-1:0], ..., a_m[n-1:0] \in \{0,1\}^n$.
   - Outputs: $s_1[n-1:0], ..., s_m[n-1:0] \in \{0,1\}^n$.
   - Functionality: For every $i \in \{1, \ldots, m\}$:

$$\langle s_i[n-1:0] \rangle = \sum_{j=1}^{i} \langle a_j[n-1:0] \rangle \pmod{2^n}.$$

   (a) Consider the task of computing $s_m[n-1:0]$. Design a cheap and fast combinational circuit that computes $s_m[n-1:0]$. Prove the correctness of your design.
   (To get full credit the delay of your design should be $O(\log(Nam))$, and the cost should be $O(nm)$).

   (b) Consider the task of computing all the m partial sums $s_i[n-1:0]$, for $i \in \{1, \ldots, m\}$. Design a cheap and fast implementation of *Partial_Sums*(n, m). Prove the correctness of your design.
   (To get full credit the delay of your design should be $O(\log(nm))$, and the cost should be $O(nm)$).

   (c) Prove a lower bound on the delay and cost of an implementation of *Partial_Sums*(n, m). You may assume that the fan-in and fan-out of every gate is bounded by a constant.

2. Let Y_1 and Y_2 denote two synchronous circuits. Let $IN_i[a_i - 1:0]$ and $OUT_i[b_i - 1:0]$ denote the input and output, respectively, of Y_i. Assume that $a_0 = b_1$ and $a_1 = b_0$.

   Let Y denote the circuit obtained by connecting the output of Y_1 to the input of Y_0, and connecting the output of Y_0 to the input of Y_1. The following figure depicts Y.

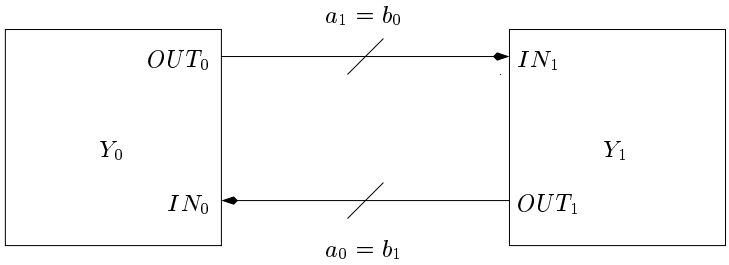

Figure 1: The circuit Y obtained from Y_1 and Y_2

   (a) Prove or disprove the statement: Y is a synchronous circuit.

   (b) Assume that Y is synchronous. Prove or disprove: There exists a real function f (independent of Y_0 and Y_1) such that for every Y_0 and Y_1

$$\Phi^*(Y) \leq f(\Phi^*(Y_0), \Phi^*(Y_1)).$$