Introduction to Digital Computers - Spring 2001

Assignment No. 10

Course homepage: http://hyde.eng.tau.ac.il/Digital_Computers01/

Firm Deadline: June 7th - before the beginning of the lecture

Remark: In these questions control signals are signals that are not transmitted along the data buses.

1. Consider the shifter environments SHenv and SH4Lenv in the DLX datapath. A shift is characterized by the following parameters:

   (a) $diff \in [0, 31]$ - the shift amount ;

   (b) $right \in \{0, 1\}$ - the shift direction ; and

   (c) $fill \in \{0, 1\}$ - the fill-bit which is zero when zeros are padded and either zero or one when the sign is extended.

   The shifters deals with three types of shifts: shift instructions, shift before store, and shift after load.

   For each type of shift specify which of the shifter environments handle the shift and how the control computes the shift parameters. Justify the equations you write.

2. Consider the ALU environment in the DLX datapath. The ALU performs the following tasks:

   (a) addition and subtraction instructions (with a two's complement adder/subtractor);

   (b) increment PC;

   (c) effective address computation;

   (d) logical instructions (bitwise and, or, and xor); and

   (e) comparisons for test-set instructions.

   Show the control signals cause the ALU to perform the right task. Specify the required control signals and justify your equations.

3. Consider the computation of the effective address for accessing the memory in the DLX:

   $$\text{effective address} = RS1 + Sext(Imm)$$

   We defined this computation formally as follows:

   $$\langle ea[31:0]\rangle = \langle R_{\langle RS1\rangle}[31:0]\rangle + \langle Sext(Imm[15:0])\rangle (\text{mod} 2^{32}).$$

   Namely, the 32 bits of $RS1$ and $Sext(Imm)$ are fed into a 32-bit adder, and the 32 bits of the sum are used as the effective address.

   Consider the following definition:

   $$[ea'[33:0]] = \langle R_{\langle RS1\rangle}[31:0]\rangle + [Imm[15:0]]$$

   (a) Why does ea' require 34 bits?

   (b) Define all the cases in which $ea[31:0] = ea'[31:0]$. Prove that you covered all the cases.

   (c) It seems that the definition of $ea'[33:0]$ is the natural definition. What would you suggest to do if $[ea'[33:0]] \neq \langle ea[31:0]\rangle$? What does the DLX do in such cases? Can you explain why the DLX does not do what you suggested?