Introduction to Digital Computers - Spring 2001
Assignment No. 5
Course homepage: http://hyde.eng.tau.ac.il/Digital_Computers01/

Firm Deadline: April 30th - before the beginning of the lecture

1. Consider the array multiplier depicted below. Describe the functionality of the "circles". Prove the correctness of the design. Extend the design to handle multiplication of numbers encoded in two's complement. Prove the correctness of your extension. Apply the extension to adding partial products in logarithmic time (using 4:2-adders and the divide-and-conquer addition tree).

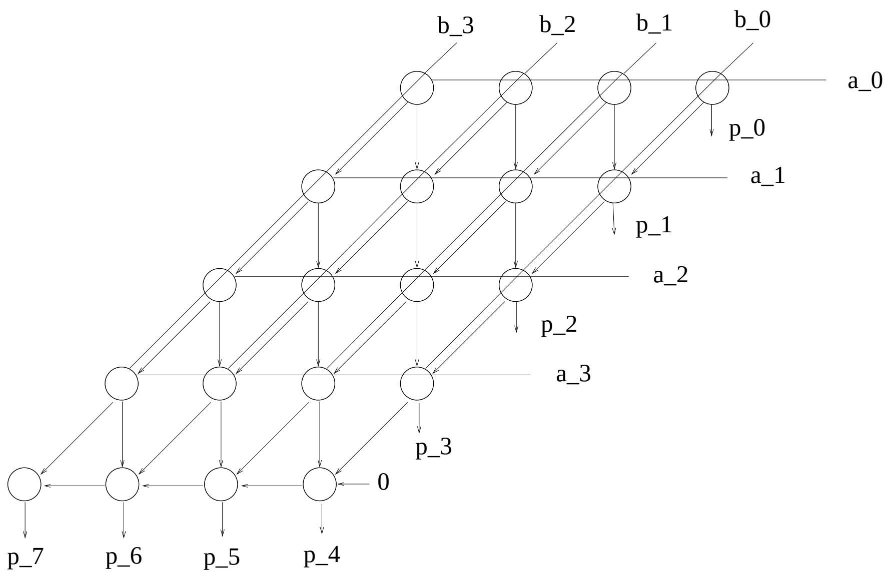

Figure 1: array multiplier - unsigned numbers

2. Consider a gate G that consists of two cascaded inverters. Suppose that $t_{pd(G)} > t_{cont}(G) > 0$ and that $t_{su}(FF), t_h(FF) > 0$.

   (a) Show how G together with a FF can be used to build a new Flip-Flop, called FF', for which $t_h(FF') < 0$. Write all the characteristics of FF' in terms of those of FF and G (i.e. setup time, contamination delay, and propagation delay).

   (b) Show how G together with a FF can be used to build a new Flip-Flop, called FF'', for which $t_{su}(FF'') < 0$. Write all the characteristics of FF' in terms of those of FF and G (i.e. hold time, contamination delay, and propagation delay).

3. In the definition of synchronous circuits, we required that the clock signal feed only the clock ports of flip-flops. Consider the circuit depicted in Figure 2 that violates this requirement. Proper functioning of the D-FF (and hence the circuit) is guaranteed only if setup and hold time requirements are satisfied. Under which conditions can the signal feeding the D port of the D-FF satisfy the setup and hold time requirements?

4. In the definition of synchronous circuits, we required that the clock ports of flip-flops be fed only by the clock signal. Consider feeding the clock port of a D-FF by combinational logic.

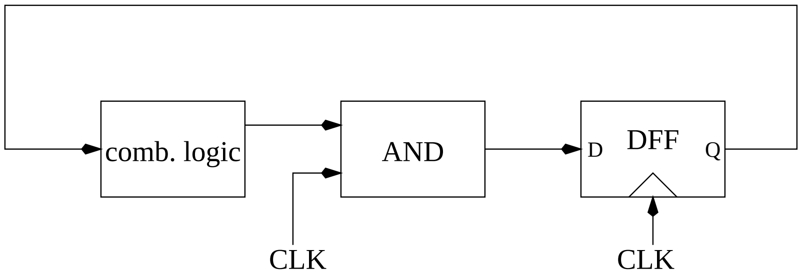

Figure 2: A "synchronous" circuit in which the clock feeds also a gate.

Obviously, glitches (i.e. non monotonous transitions between logic levels for periods of time that are shorter than the propagation delay) can cause errors in such a situation because glitches might cause unwanted "rising edges". Consider the circuit depicted in Figure 3 in which a "glitch-free" combinational circuit feeds the clock port of the D-FF. Assume that the output of the glitch-free circuit changes from time to time (perhaps its input vary over time). Proper functioning of the D-FF (and hence the circuit) is guaranteed only if setup and hold time requirements are satisfied. Under which conditions can the signal feeding the D port of the D-FF satisfy the setup and hold time requirements?

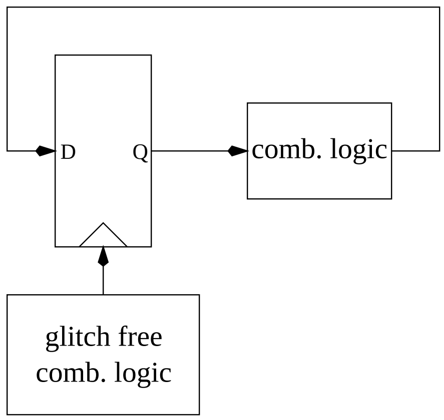

Figure 3: A "synchronous" circuit in which combinational logic feeds the clock port of a D-FF.