Introduction to Digital Computers - Spring 2001

Assignment No. 6

Course homepage: http://hyde.eng.tau.ac.il/Digital_Computers01/

Firm Deadline: May 7th - before the beginning of the lecture

1. Recall the table filled in class in which we specified the intervals where signals should be stable. Extend this table to the general case where we cannot assume that: $t_h(FF) < 0, t_{cd}(FF) = 0$.

2. Let S denote a synchronous circuit in which all the flip-flops have the same critical interval, C, and the same interval, A, in which the output may change. Prove: if $A \cap C$ is empty, then there exists a minimum clock period Φ^* such that, for every clock period $\Phi \geq \Phi^*$, the circuit S functions properly. Note that you should give a formal proof that would apply for all possible values of $t_h(FF), t_{cd}(FF)$.

3. Consider a synchronous circuit with control, S, (consisting of gates, flip-flops, memories, drivers, and nets).

   (a) Write an algorithm for determining the minimum feasible clock cycle Φ^* of S.

   (b) Prove the correctness of your algorithm. You may rely on the algorithm for computing the minimum feasible clock cycle of a synchronous circuit.

   (c) What is the complexity of your algorithm?