Sheet1

lecture no.	HW	date	topic
1-2		05/3	Combinational Circuits: definitions, simulation theorem, delay and cost
3-4	1	08/3	Vector Notation, Combinational Modules I (half-decoder, decoder, OR-tree, zero tester)
5-6		12/3	Combinational Modules II (encoder), Ripple-carry adder, Carry Bits, Adder II (divide \& conquer, cond
7, T1	2,S1	15/3	carry-bits, divide & conquer addition
8-9		19/3	cond-sum adder, parallel prefix adder (I)
10, T2	3,S2	22/3	parallel prefix adder (2)
11-12		26/3	signed addition: two's complement, reduction of two's complement addition to unsigned
13-14	4	29/3	multiplication: arrays and trees
T3-T4	S3+?	02/4	
15-16		16/4	Synchronous Systems: semantic definition, clock, zero-propagation model, D-latch, edge-triggered FF
17,T5	5,S4	19/4	Synchronous Systems: syntactic definition, functionality, timing constraints
18-19		23/4	Synchronous Systems: syntax & semantics, timing verification, contamination delay, clocks & clock sk
20,T6	6,S5	30/4	Synchronous Systems: using the negated clock to speed up computation
21-22		03/5	More components: drivers, memories. Busses: protocol, controller, master, slave
23-T7	7,S6	07/5	Sequential Circuits: defintions and proper functionality.
24-25		10/5	DLX: introduction, instruction set
26,T8	8,S7	14/5	DLX: instruction exeution flow I
27-28		17/5	DLX: instruction execution flow II, control and datapath
29,T9	9,S8	21/5	DLX: control & datapath
30-31		24/5	Interrupts: Introduction I
32,T10	10,S9	31/5	Interrupts: intorduction II
33-34		04/6	Interrupts: hardware and software support I
35,T11	11,S10	07/6	Interrupts: hardware & software support II
36-37		11/6	Interrupts: correctness proof
38,T12	S11	14/6	Interrupts: extensions
			homework topics
			shifters
			Synthesis of FSM
			DLX: instruction set
			DLX: implementation of datapath

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