Computer Structure Lab - Fall 2001
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Handout #1: The RESA's Backplane Bus

Quiz on Nov. 1st on Resa Bus & Bus Slave

Submission deadline: beginning of 3rd lab meeting.

Consider a CPU that wants to communicate over the RESA bus as a master device. The CPU is connected to the RESA bus via a simple bus interface. The simple bus interface is placed on the CPU board between the CPU and to the RESA bus. Communication between the CPU and the bus interface is implemented by 3 registers and 3 control signals. The functionality of the registers is as follows:

$R0$**:** a data-in register through which data is fed to the CPU.

$R1$**:** a data-out register through which data is sent from the CPU.

$R2$**:** an address register that is written by the CPU.

The control signals are as follows:

`rd_req`**:** a signal sent by the CPU to the bus interface. This signal indicates that the CPU wishes to initiate a read transaction.

`wr_req`**:** a signal sent by the CPU to the bus interface. This signal indicates that the CPU wishes to initiate a write transaction.

`done`**:** a signal sent by the bus interface to the CPU. This signal indicates the completion of a transaction.

For example, a read transaction is implemented as follows: When the CPU wishes to read data from a slave, it writes the address (combined addresses of the slave and the data item) to the address register $R2$ and sets the `rd_req` signal to "1". The bus interface, handles the request, and initiates a read transaction over the RESA bus. When the data is fetched, it is stored by the bus interface in the data-in register $R0$, and the `done` signal is set to 1 for one clock cycle. The CPU will then immediately change the `rd_req` signal back to "0".

1. Describe how a write transaction takes place.
2. Draw the datapath, registers, and drivers of this bus interface.
3. Design the control logic of the bus interface. Write the equations for: the register clock enable signals, the output enable signals of drivers, and all the RESA bus signals. Use active low signals for all the signals that require a wired-OR mechanism.
4. Draw the timing diagram of all the signals described above in the bus interface for a read transaction and a write transaction.

5. Project "ex1" in the lab contains 4 macros: a CPU, a Bus Interface, a Bus Controller, and a Slave. The CPU alternates between read and write transactions. Your task is to design the Bus Interface macro.

   Remarks: (a) The Bus Controller is very simple. It returns a bus grant for every bus request. (b) The Slave only returns an `ack` signal. This means that the Data signals on the RESA bus are completely ignored both by the Slave and by the CPU.

   (a) Design the Bus Interface macro (design entry). Submit a printout of your schematics and VHDL programs.

   (b) Simulate the project using the following input waveforms: a 100ns period `clk` and a `reset` pulse of duration 200ns. Submit a printout of your simulation for a read transaction and a write transaction.