Computer Structure Lab - Fall 2002
Dr. Guy Even

Handout #4: A Read Machine and A Write Machine

1 Pre-lab Assignment

(submit in the beginning of the 6th lab meeting)

1. (20 pts) Design a Read Machine and a Write Machine. Submit hand-written designs.
2. (10 pts) Suppose that we wish to monitor the activity of a Read Machine using the Logic Analyzer module. We would like to start sampling when the `STEP_EN` signal rises, and end the sampling two cycles after the Read Machine returns to the "wait" state. Write the equations for the following signals:
   (a) Write enable (`WE`) signal of Logic Analyzer's RAM.
   (b) Count enable (`CE`) signal of the Logic Analyzer's counter.
   (c) The reset signal of the Logic Analyzer's counter.

   Remark: Make sure that, after an active `reset` signal generated by the I/O Control Logic, the Logic Analyzer is properly initialized. This means that, after a reset, the first sampling session functions correctly.
3. (5 pts) Same question for the Write Machine.
4. (5 pts) Is it possible to design a modified Read Machine that has the same functionality but does not have the "load" state? Can you also get rid of the "terminate" state in the Write Machine?

2 Post-lab Assignment

(submit in the beginning of the 7th lab meeting) (60 pts)

1. Prepare two designs:
   (a) A design with the I/O control logic, the Monitor Slave (with the Logic Analyzer), and the Read Machine.
   (b) A design with the I/O control logic, the Monitor Slave (with the Logic Analyzer), and the Write Machine.
2. Implement your designs on the RESA.
3. Prepare a configuration file for the PC monitoring program, and execute your design.

4. Submit: printouts of design, simulation and monitoring results of: (a) the state transitions; (b) the bus activity of the machines; and (c) the accessed memory address (In the Read Machine, this means that the register of the Read Machine is monitored as well as the main memory address. In the Write Machine, only the main memory address is monitored).