Computer Structure Lab - Fall 2002

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`http://hyde.eng.tau.ac.il/Resa02/resa_home.html`

Quiz on October 17th on the Resa backplane bus

Handout #0: The Xilinx Foundation Software

The assignment in this lab is to practice design entry (schematic and VHDL) and simulation on a design which is fully given to you. Please do not submit your work. It will be assumed that you have successfully completed it within a week.

Detailed Instructions:

We want to draw a project which is identical to the `decoder` project which already exists in your PC filesystem. You may view the `decoder` project to see what your design should look like. Start Xilinx Foundation application. The project consists of a counter (designed using VHDL), an AND-gate, and a FLIP-FLOP. The decoder design (which uses a counter, gate, and flip-flop) is designed using schematic entry. A printout of the project appears in the end of this writeup.

Activate the simulator. Choose the signals using the menu option Signal → Add_Signals. In the "Chip Selection' window, double click to select the chip, then double click on the block the signals of which you want to select, and then on the right hand window, double clock to select the signals you want to watch. Choose the following signals:

1. Inputs: `CNT, RESET, CLK`
2. Outputs: `CNTOUT[3:0], PULSE_C-F, PULSE_D-0`.

The stimulators (the input waveforms) are set in two stages. First, formulas are written. Then, each formula is matched with an input signal. Formulas are defined by selecting the menu option Signal_Add_Stimulators, and tapping the Formula Button, followed by double clicking the requested formula, typing the formula in the bottom row, and pressing Accept. Use the following formulas:

1. `f0 = L101H` to stimulate `CNT`. This means: Low for 101ns, then High forever.
2. `f1 = L2001H` to stimulate `RESET`.

The Clock signal `CLK` is driven by using `b0` (this is simply a zero-one alternating signal). The matching between formulas and signals is done by selecting the signal and then selecting the corresponding formula.

Note that the input signals transition only between clock ticks. The clock ticks occur in multiples of 100ns, and this is why the input signals change 1ns after the clock transition.

Run the Simulation. The default presentation depicts the values of the busses in hexa-decimal, but in reverse order (MSB on the right). A reverse interpretation of bus values is obtained by selecting the signal from the left window, and then choosing the menu option Signal → Bus → Change_Direction. Change the direction of the `CNTOUT` bus.

Make sure that you understand the difference between the pulse output signals.