Computer Structure Lab - Fall 2002
Dr. Guy Even

Handout #3: Built-In Self Monitoring

1 Pre-Lab Assignment

hand-in the pre-lab assignment in the beginning of the 5th lab meeting
Consider an application of a 5-bit counter which alternates between two modes: counting down from 20 to 0 (staying with 0 until the next step-enable signal) and counting down from 10 to 0 (staying with 0 until the next step-enable signal). A step-enable signals causes the counter to reset and start counting. Our goal is start sampling the state of counter starting with rising edge of the clock that occurs after the rising edge of the step enable signal. The sampling should stop when the counter is "stuck". The application generates a signal called `in_init`. When `in_init` is high, the counter's value equals 0 (i.e. the counter is "stuck" and sampling by the Logic Analyzer should stop).

1. (5 pts) Which control signals should the application transmit to the Monitor Slave (including the Logic Analyzer)? Differentiate between signals that are monitored by the Logic Analyzer, and signals that aid the Monitor Slave and the Logic Analyzer in functioning properly.

2. (10 pts) Write the equations for the following signals:

   (a) Write enable (`WE`) signal of Logic Analyzer's RAM.

   (b) Count enable (`CE`) signal of the Logic Analyzer's counter.

   (c) Clock enable (`CE`) signal of the Status Register.

   (d) The reset signal of the Logic Analyzer's counter.

   (e) The Select signal of the mux that selects the address input of the Logic Analyzer's RAM.

3. (25 pts) Extend the Slave design from the previous handout to support (a) read transaction from the Status Register; (b) read transactions from the Logic Analyzer's RAM; (c) write transactions to the Command Register. Submit a hand-written design.

   Remark: a configuration file for the RESACTRL program will be posted on the lab's web-site. Use the same addresses that appear in that configuration file so that your design is compatible and to simplify comparison of the monitored wave-forms.

2 Lab Assignment

submit in the beginning of the 6th lab meeting.

1. Implement, configure, and run project "ex3" on the RESA. Monitor the states of the counter and verify that it functions properly.

2. (60 pts) Replace the Monitor Slave macro in project "ex3" with your own design. Submit printouts of your design, simulation wave forms, and wave forms monitored by the RESACTRL program.

Warnings and reminders:

1. **This exercise requires using the RESA. Do not touch it! The RESA is connected to the PC and all the operations should be done via the PC control program (including reset).**

2. **Do not use drivers in your design!!! Conflicting drivers (due to design errors) can cause hardware damages.**

3. **Follow the following design rule: All registers should be clocked by the same clock. The registers differ in the clock enable signals.**

4. **You will need your Monitor Slave design for all your future lab assignments. Spend some extra time making sure it is well designed.**