Computer Structure Lab - Fall 2003

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Handout #2: A simple slave device

Submission deadline: beginning of 4th lab meeting.

Guidelines for the whole lab

Do not use tri-state buffers (i.e. drivers) at all in your designs!!! The justification for this is that a conflict of drivers may cause electrical damages to the circuit. Use MUXs instead of buffers.

When you start the project (with the Xilinx software) specify the type of FPGA you will be using as: XC 4025 HQ240 speedgrade 2.

1. Design using VHDL a 32-bit binary counter and simulate the counter. The counter should have the following inputs and outputs:

   (a) `clk`: the clock;

   (b) `ce`: the clock enable, when high the clock is enabled, when low the clock is ignored;

   (c) `reset`: resets the counter value to zero;

   (d) `cnt`$[0:31]$: the output counter value.

   The functionality of the counter is as follows.

   (a) A clock pulse P is enabled if the clock enable signal is high during the duration of P.

   (b) A reset signal is caught in time t if: (a) `reset`$(t) = 1$; (b) `ce`$(t) = 1$; and (c) the clock undergoes a rising transition in time t.

   (c) Let $\delta(t_0, t_1)$ denote the number of rising edges of enabled clock pulses that occurred in the interval $(t_0, t_1]$.

   (d) Consider a time t. The time $t_{\texttt{reset}} \leq t$ is defined as the last time in which a reset was caught.

   (e) The binary number represented by `cnt`$[0:31]$ in time t equals $\delta(t_{\texttt{reset}}, t) \bmod 2^{32}$.

   (f) Bonus: think about the following point: how can you make the counter faster (i.e. shorten the clock period of the counter so that the clock period is O(1) instead of O(n))? Take into account that this is not a general adder.

2. Design the slave device. The slave is connected to the `cnt`$[0:31]$ output of the counter.
3. Build a library component consisting of: the I/O control logic, the 32-bit binary counter, and the slave device.
4. Prepare a configuration file for the PC monitor program. Run your design on the RESA with the PC monitor program.
5. Submit your lab report one week later. Print your designs, configuration file, and simulations.